Docket No.: M4065.0743/P743
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Steven T. Harshfield, et al.

Application No.: 09/853,233 Group Art Unit: 2823

Filed: May 11, 2001 Examiner: William D. Coleman

For: PCRAM MEMORY CELL AND METHOD OF MAKING SAME

DECLARATION OF TERRY L. GILTON CALLING ATTENTION TO INFORMATION PURSUANT TO 37 C.F.R. § 1.56

Commissioner for Patents
Washington, DC 20231

Dear Sir:

I, Terry L. Gilton declare and state as follows:

1. I reside at 3149 E. Nature Dr., Boise, ID 83706.

2. I am a project manager at Micron in charge of research and development of new memory devices based on variable resistance materials such as doped chalcogenide glass, including the subject matter disclosed and claimed in the above-captioned application. I have held this position since April, 2000.

3. Micron Technology, Inc. ("Micron") is the assignee of the invention claimed in the application identified above.

4. I am making this Declaration in order to bring to the attention of the Patent and Trademark Office information which may be deemed material to the prosecution of this application.

5. To my best information and belief, on March 22, 2000, Micron entered into a Research and License Agreement ("Agreement") with Axon Technologies Corp. (Axon) and Michael Kozicki ("Kozicki"), pursuant to which Axon and/or Kozicki would perform certain research on behalf of and provide information to Micron with respect to Programmable Metallization Cell Technology ("PMC Technology"), which is based on metal-doped chalcogenide materials.

6. To my best information and belief, pursuant to the Agreement, the requirement by Micron to keep information received from Axon and/or Kozicki confidential has now expired.

7. Pursuant to the Agreement, on April 6, 2000, Kozicki, an employee of Axon and a professor at Arizona State University ("ASU"), gave a presentation to several members of my project team on the topic of PMC. I was also present at this presentation. Copies of a handout and slide show from this presentation are attached as Exhibit 1. A PMC cell structure employing an "active-in-via" arrangement is disclosed in section 1.3.1 and Fig. 1 of the handout and page 5 of the slide show.

8. Pursuant to the Agreement, on or about September 5, 2000, Axon also sent Micron several Kozicki invention disclosures, one of which was entitled "Programmable Metallization Cell With Floating Electrode," and identified as M1-008. A copy of the cover letter forwarding the disclosures is attached as Exhibit 2, while a copy of the invention disclosure is attached as Exhibit 3. A PMC cell structure with a floating electrode is disclosed on pages 4-5 of Exhibit 3.

9. To the best of my knowledge, the subject matter described in Exhibits 1-3 was not disclosed in any publication or otherwise publicly disclosed prior to the respective dates they were delivered to Micron.

10. The information disclosed in the attached Exhibits may or may not be "material" pursuant to 37 C.F.R. § 1.56. The disclosure of this information is not intended as an admission that it is material or that it constitutes prior art with respect to the invention claimed in the above-captioned application.

11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information or belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this declaration, the present application, or any patent resulting therefrom.

10/9/03
Date

Terry L. Gilton, Phd.

Michael N. Kozicki
February 18, 2000

1. PROGRAMMABLE METALLIZATION CELL TECHNOLOGY DESCRIPTION

1.1 INTRODUCTION

It is well known in the field of electrochemistry that metals such as silver or copper can be dissolved in chalcogenide glasses such as arsenic sulfide or germanium selenide, to form solid solutions. These solid solutions are relatively poor conductors, with resistivity in excess of 10^8 times higher than that of the solid metal, as conduction is dominated by ion transport through the solid electrolyte. If electrodes are formed in contact with a layer of the solid solution and a voltage is applied between them, the positively charged metal ions will migrate toward the cathode region. Under appropriate conditions, the ions will come out of solution at the cathode to form a stable metallic electrodeposit which may be made to extend from the cathode to the anode. The electrodeposit can form on the surface of the chalcogenide or through a thin layer of the glass, depending on the placement of the electrodes. In either case, the low resistance metal electrodeposit acts to short-out the relatively high resistance glass and hence the overall resistance of the structure can be reduced by many orders of magnitude via this electrically-stimulated deposition process. This is the basis of the Programmable Metallization Cell (PMC) technology [1]. In our work to date, we have concentrated on arsenic sulfide-silver (As_2S_3-Ag, AsS_2-Ag) and germanium selenide-silver ($GeSe_2$-Ag, Ge_3Se_7-Ag) systems [2]. We have also investigated copper as the dissolved metal species.

1.2 FUNDAMENTAL MECHANISMS

The metal may be added to the chalcogenide by thermal diffusion or by photodissolution to create a ternary source for physical vapor deposition or after the glass is deposited as a thin film on the substrate. The photodissolution process involves the illumination of a metal/glass bilayer with light of energy greater than the optical gap of the chalcogenide [3]. The amount of metal dissolved in the film depends on the initial thickness of the metal layer and the illumination dose. The photodissolution of the metal is thought to result in the reduction of the cation in the film and the process is therefore self-limiting, halting when the cation has been reduced to its lowest oxidation state [4]. For silver in arsenic trisulfide, this occurs at a ternary composition of $Ag_4As_2S_3 = 2Ag_2S + As_2S$ with a corresponding silver concentration of 44.4 atomic %. This concentration has been confirmed in our films using Rutherford Backscattering Spectrometry (RBS) [2]. Note that if the metal is thermally dissolved into the chalcogenide, the saturation concentration may be higher than in the case of photodissolution [2]. Dissolved metal concentration may be maintained in the film even as metal comes out of solution during electrodeposition if there is a source of the same metal at the anode. The metal from the anode dissolves into the glass and moves toward the growing electrodeposit by a coordinated motion of the ions. This replacement of metal appears to be necessary for rapid and stable electrodeposit formation for the reasons discussed below.

The electrochemical deposition of metal from solid solutions has been reported by other researchers in the past [5–8] but a complete understanding of this solid phase growth process has been somewhat elusive. The deposition of metal at the cathode and partial dissolution of the same metal at the anode indicates that device operation is analogous to the reduction-oxidation electrolysis of metal from an aqueous solution. When an electrical bias is induced across an electrolytic cell, the anode will oxidize if the oxidation potential of the metal anode is greater than that of the solution. Under steady state conditions, as current flows in the cell, the metal ions will be reduced at the cathode. For a solid solution of metal ions (M^+), this reaction may be represented by:

$$\text{Anode: } M \rightarrow M^+ + e^-$$

$$\text{Cathode: } M^+ + e^- \rightarrow M.$$

The electrons are supplied by the power source to the cathode and flow in the external circuit. When a potential is applied across the electrodes, metal ions migrate from the anode toward the cathode under the driving force of the applied electrical potential and the concentration gradient. This ion transport through the electrolyte will be the rate-limiting factor in the electrodeposition process if the electrodes are widely spaced but is much less of a factor in sub-micron structures. At the boundary layer between the electrolyte and the electrodes, a finite potential difference exists due to the transfer of charge and change of state associated with the electrode reactions. This potential difference leads to polarization in the region close to the phase boundary (the electric double layer). When an external voltage is first applied across the electrodes, "non-Faradaic" current will flow in order to charge the double layer, without causing any reduction or oxidation of the metal. An important consequence of the electric double layer is that for the redox reaction to proceed, the applied potential must overcome this double layer potential. There is therefore a "threshold voltage" for electrodeposition, below which no metal deposition occurs. For all practical purposes, this voltage is in the order of a few hundred millivolts for the metal-chalcogenide structures described above.

If the anode is replaced with a metal with a lower oxidation potential than the solid solution, the anode will be essentially chemically inert and only serve as an electronic conduction path. The reduction of the metal ions in solution at the cathode will then occur at the expense of the solution. The concentration of metal ions in the solid solution will decrease during electrodeposition on the cathode until the electrode potential equals the applied potential and reduction will then be halted. Further reduction requires greater applied voltage (governed by the Nernst equation), so that the electrolytic deposition process is self-limiting for a moderately low applied potential. This has important consequences for device operation as the "stalled" electrodeposit may not bridge the electrode gap and hence the resistance of the device will remain high. In addition, the metal depleted glass could result in the subsequent thermal dissolution of the electrodeposit, which would not occur if the glass was maintained at the metal saturation point through dissolution of a silver anode.

Finally, it should be noted that the electrodeposition is reversible by the application of a reverse bias. If the electrodeposit itself is made the anode, it will dissolve back into the chalcogenide as metal comes out of solution at the opposite electrode. In devices which consist of a thin film of the solid solution in a via hole between the electrode layers, the metal will tend to redeposit in the area from which it came as this zone will be slightly depleted of metal by the original electrodeposit growth. In any device configuration, the magnitude of the field will have

an effect on electrodeposit morphology; low fields will tend to produce a "densely branched" relatively flat deposit on the electrode whereas higher fields will produce elongated "diffusion limited aggregate" structures [9]. It is important to avoid this latter type of deposition in the reverse bias case if the intent is not to grow a bridging electrodeposit so that we may break or "erase" the connection between the electrodes.

The electrical characteristics of the PMC metal/solid solution/metal arrangement are complex but may be represented by a number of models. The a.c. equivalent circuit modeling which was performed by our group has been described elsewhere [10] but the small-signal "off" characteristics of the device are dominated by the electric double layer and are therefore somewhat similar to a metal-semiconductor or "Schottky" contact. This means that prior to electrodeposition, the current increases exponentially with applied voltage. Once the electrodeposit forms, the device looks very much like a metal wire with ohmic (linear current-voltage) characteristics as the double layer and solid solution is effectively shorted out by the metal element.

1.3 DESCRIPTION OF THE DEVICE TECHNOLOGY

1.3.1 Structure

The preferred configuration is the "active-in-via" (AIV) variant of the PMC technology. This device configuration has the solid solution of metal ions in chalcogenide wholly contained within a via hole in a dielectric layer. This is an extremely compact structure and lends itself well to scaling. Indeed, we have been able to demonstrate the operation of AIV devices in vias as small as 50 nm in diameter and there should be no reason why these devices should not be able to be scaled to the sub-10 nm regime. The best materials for the dielectric from the viewpoint of containing potential mobile ion contamination are silicon nitride, silicon oxynitride, or polymeric materials such as polyimide or parylene-n. The solid solution has an excess of the dissolved metal, e.g. silver or copper, in the form of a thin film on one of the contact surfaces (top or bottom). If photodissolution is used to form the solid solution, more metal than is required to saturate the solution is initially deposited so that when dissolution is completed, a thin layer of excess metal remains. The connections to the top and bottom surfaces of the solid solution/metal bilayer are made from the interconnect layers above and below the dilelectric layer. The interconnect material in direct contact with the solid solution should be indifferent, i.e., not electrochemically active. For example, copper, silver, or zinc should not be used but tungsten, nickel, molybdenum, platinum, various common silicides, etc. are acceptable. If this interconnect layer is formed from an active material, a barrier layer, such as titanium nitride, should separate the solid solution from the metal. The structure for the case of Ag in Ge_3Se_7 is shown schematically in Fig.1. Note that for this device configuration, the electrodeposit will actually form on the surface of the solid solution which is in contact with the surrounding insulator, i.e., at the interface between the chalcogenide and the dielectric.

1.3.2 Write operation

The off resistance of the device shown in Fig. 1 depends on a number of factors, including geometry and processing history, but can readily be well in excess of 1 MΩ. When a forward bias above the electrochemical threshold voltage is applied to the device - positive to the excess metal electrode, negative to the indifferent electrode - significant outward growth of an electrodeposit will occur from the indifferent electrode. Electrodeposition will initially tend to

occur at the point where the electric field is highest, e.g., at an asperity or "rough point" at the electrode, but once an electrodeposited "bud" has formed, all subsequent deposition will take place at the tip of the growing electrodeposit as this is the point at which the electric field remains the highest. This extended electrodeposit will bridge the gap between the electrodes and hence the resistance will drop by many orders of magnitude. On the other hand, a reverse bias prior to any electrodeposition will result in a non-extending electrodeposit on the negative electrode and hence the resistance will not change by any significant amount (it actually increases slightly due to depletion of ions in solution). The time it takes to form the link depends on the applied current and the volume of the electrodeposit, the latter determining the link resistance. In the calculations of switching speed, we assume the following:

(a) The electrodeposition process is 100% efficient - every electron results in the deposition of one atom in the link. Since $N_{Ag} = 5.8\times10^{22}$ atoms/cm^3, the total charge required per cm^3 of electrodeposit = 9.28×10^3 C.
(b) The electrodeposit has a uniform cross-sectional area, A, and the thin film resistivity, ρ, is 100× (worst case) the bulk value for silver (i.e., $100\times1.5\times10^{-6}$ Ω.cm). The electrodeposit resistance can therefore be calculated from $R = \rho L/A$ where L is the length of the device.
(c) We can ignore parasitics such as double layer capacitance and electrodeposit contact resistance.

For a 0.25 μm diameter device with a 30 nm thick solid solution in the via ($L = 3\times10^{-6}$ cm), if we wish to produce a connection resistance R which is in the order of 1 kΩ, $A = \rho L/R = 4.5\times10^{-13}$ cm^2. For $L = 3\times10^{-6}$ cm, the electrodeposit volume is 1.35×10^{-18} cm^3. The total charge required to form this 1 kΩ connection is 1.25×10^{-15} C. This suggests that a constant applied current of 1 μA should allow switching in the nsec regime, although parasitic capacitances will tend to increase this time. Since the voltage required to drive this current can be in the order of a few volts, even accounting for inefficiencies the energy used is significantly less than 1 pJ to reduce the resistance of the device by several orders of magnitude.

The growing electrodeposit progressively harvests the ions from the entire length of the solid solution as it grows from the cathode to the anode. This is an important point as it means that the ions which ultimately form the metallic link only have to move a short distance from just below the surface of the solution (ion movement is normal to the growth) in order to join the electrodeposit at its tip. If we assume that the electrodeposit thickness in a typical active-in-via device is around 1 nm, the depth of solid solution required to supply ions for this is around twice this thickness which means that the ions only have to migrate at most a few nm. This, coupled with the high electric fields present (around 10^6 V/cm) means that the electrodeposition process can be extremely fast. Exactly how fast will be largely determined by the mobility of the ions in the solid solution. For example, if the ion mobility is around 10^{-5} cm^2/V.sec (which, for comparison, is over a hundred million times less than electron mobility in silicon at room temperature), the ions would only take around 20 nsec to move from the solid solution to the growing electrodeposit. Although there are currently no values published for silver ion mobility in silver-germanium selenide ternaries, available results suggest that mobility will be in excess of 10^{-5} cm^2/V.sec [11]. This would allow PMC devices to perform at speeds which are close to current DRAM performance.

1.3.3 Mobility and device speed enhancement

The electrochemical process on which the Programmable Metallization Cell technology is based involves the electrodeposition of metal from a solid solution. The metal in solution is in ionic form and will move under the influence of an electric field as long as the structure of the metal-chalcogenide material allows the ions to be mobile at room temperature. For example, amorphous or "glassy" compounds, phase-separated materials, and polycrystalline films may support ion movement due to the relatively "open" nature of their structures, i.e., they all contain defect-rich regions which can act as pathways for ion drift under an electromotive force.

The key to creating a fast device is to ensure that the ion mobility is made as high as possible. One way of doing this is to add a material which deliberately "weakens" the structure of the solid solution, creating more defects and therefore allowing the ions to move more easily under the influence of an electric field. The halogens seem to work well in this respect; iodine is known to reduce the glass transition temperatures of chalcogenides (an indication of structural change) and ion mobility is seen to increase significantly. It is also possible that hydrogenation of the chalcogenide and the addition of other network modifying elements will produce the same effect (e.g. Ag in selenium-rich Ge_xSe_{1-x} is known to be a network modifier).

1.3.4 Threshold voltage control

For most low power/high density memory applications, the extremely small switching threshold voltage of the metal-chalcogenide structure is ideal. Fig. 2 shows the characteristics of a device which switches from its high resistance state (around 7.5 MΩ at 100 mV) to a low resistance value of 20 kΩ (determined by the current limit – see later) at a write voltage, V_W, of 180 mV. However, in applications such as anti-fuses and some memory configurations, a write voltage higher than a few hundred millivolts may be desirable. This is possible by incorporating an electrically insulating "barrier" material on the cathode which prevents a complete connection between the electrodes via the electrodeposition process. This barrier must be thin enough to allow electrons to tunnel from the cathode conductor through to the solid solution and thereby promote electrodeposition on the barrier material itself but thick enough to limit the tunneling current at low voltage so that the off state is maintained even when an electrodeposit has been formed. One example of a suitable barrier is that created by the oxidation of the cathode material; indeed, a native oxide, grown spontaneously in air to a self-limiting thickness of a few nm, may be sufficient for this purpose. As an alternative, a different barrier material may be formed on the cathode using an appropriate growth or deposition technique. With the incorporation of a barrier such as this, the device will not switch to its low resistance state until the voltage-drop across the barrier region exceeds the breakdown value for the barrier material. Breakdown voltage for oxides is typically in the order of 1 V/nm and hence a barrier thickness of 1 - 3 nm is sufficient to push the switching threshold voltage to 1 - 3 V. Figs. 3 and 4 show control of V_W by way of the incorporation of an oxide barrier on the anode. The device of Fig. 3 has an oxide barrier on its nickel anode which is in the order of 1.7 nm thick, formed by oxidation in air, and the corresponding V_W is seen to be 1.7 V. The device of Fig. 4 uses a chromium anode with a thicker native oxide (exact thickness in the device is unknown) and the corresponding V_W is above 3V in this case.

Fig. 5 shows the current-voltage (I-V) characteristics of a 4 μm via diameter test version of the device of Fig. 1. The solid solution is a 35 nm thick layer of silver/germanium selenide, doped by photodissolution to saturation. No attempt was made to remove the native oxide on the

cathode prior to the deposition of the chalcogenide and the resulting barrier thickness is thought to be in the order of 1.3 - 1.5 nm. In this particular device, the current below 0.5 V is less than 1 pA, indicating an off resistance in the TΩ region, but rises rapidly above this. This shows that the I-V characteristics are dominated by tunneling through the oxide barrier. Fig. 6 shows the I-V characteristic of the same device for forward bias (positive on top contact, negative on bottom) from zero to 2 V. At a forward bias in excess of a few hundred mV, metal will come out of solution at the cathode (lower electrode). However, if the bias is below 1 V or so, the (intact) barrier at the cathode will determine the overall device resistance; only a small tunneling current will flow and so the resistance remains high. At a forward of 1.4 V, there is sufficient voltage across the barrier to rupture it and the electrodeposit is allowed to link the electrodes. This is illustrated by the "write" curve of Fig. 6, which indicates that the device is in its low resistance (metallic or Ohmic) on state.

1.3.5 Multi-bit storage

The on state resistance is set by the amount of charge which flows during the electrodeposition process. *This holds for barrier or non-barrier devices and is independent of device geometry.* In the case of the device of Fig. 6, this resistance is in the order of 200 Ω, a change of more than nine orders of magnitude from the off state. Note that electrodeposition only proceeds if the voltage is in excess of approximately 0.2 V. The process can therefore be self-limiting by restricting the current flow such that when the resistance drops, the voltage across the device falls below this critical threshold and the electrodeposition halts, thereby fixing the resistance. This effect may be expressed simply as

$$R_{on} = 0.2/I_{lim}$$

where R_{on} is the on resistance and I_{lim} is the maximum current which is allowed to flow. The current limit for the device of Fig. 6 is 1 mA and hence the on resistance is 200 Ω but if I_{lim} is decreased to 100 μA, R_{on} will be in the order of 2 kΩ, and so on. For the devices of Figs. 2 – 4, the current limit was set at 10 μA and hence the on resistance was limited to 20 kΩ in all cases. In the simplest sense, the off and on resistance states can be used to store digital information in binary form. However, the programmable resistance effect allows us to employ more than two resistance states to represent and store information. For example, if we can program the on resistance to any one of three well defined and stable values (R_1, R_2, R_3), this plus the off state (R_0) will allow us to store two bits of information in digital form in each device, i.e.,

$$R_0 = 00$$
$$R_1 = 01$$
$$R_2 = 10$$
$$R_3 = 11$$

In practice, the limitation to the amount of information stored in each cell will depend on how stable each of the resistance states is with time. For example, if we have a programmed resistance range of 3.5 kΩ and a resistance drift over a specified time for each state of ±250 Ω, we could fit 7 equally sized bands of resistance (7 states) into this range which could be used with the off state to represent 3 bits. If the drift was dependant on the magnitude of the resistance, i.e., could be represented as a percentage of the programmed resistance, then the

overall range could be divided logarithmically, with larger bands for the higher resistances. Fig. 7 illustrates three bit storage for a three decade resistance range and a maximum drift of ±45%. In the limit, for near zero drift in a specified time limit, information could be stored as a continuum of states, i.e., in analog form.

1.3.6 Read operation

The state of the device may be read by applying a forward or reverse bias of magnitude less than the voltage threshold for electrodeposition or by using a current limit which is less than or equal to the minimum programming current (the current which will produce the highest of the on resistance values). This will ensure that the device state is not disturbed by the read condition. A current limited (to 1 mA) read operation is shown in Fig. 6. In this case the voltage is again swept from 0 to 2 V and the current rises up to the set limit (from 0 to 0.2 V), indicating a low resistance (Ohmic/linear current-voltage) state. Another way of performing a non-disturb read operation is to apply a pulse which has a voltage which could be considerably higher than the electrochemical deposition threshold but whose duration is such that no appreciable Faradaic current flows, i.e., nearly all the current goes to polarizing/charging the device and not into the electrodeposition process.

1.3.7 Erase operation/cycling

The erase operation involves the application of a reverse bias of magnitude greater than the threshold for electrodeposition. In this case, the non-symmetric nature of the device promotes reverse electrodeposition or electrodissolution, thereby returning the metal to the solution and removing the link between the electrodes. The device therefore returns to its high resistance off state. Note that if the erase voltage is lower than 1 V or so, electrodeposition on the excess metal layer will not result in a link growing from this electrode but in a "re-plating" of material in the location which supplied the metal during the previous (forward bias) electrodeposition event. Note that the charge required for the electrodissolution is the same as that originally required to grow the link and hence the erase operation is also a very low energy process. Fig. 8 illustrates the effect of a voltage sweep from 0 to –1 V. From 0 to around 0.2 V, the device is clearly on but quickly attains a high resistance state when the applied voltage exceeds this threshold. Fig. 9 compares the I-V curves of the same device before a write operation and after it has been erased. These low current/high resistance curves are very similar, indicating that the switching process is indeed fully reversible. Note that as long as the electrodeposition/electrodissolution threshold can be exceeded, the device will erase.

In both barrier and non-barrier devices, the write erase process is repeatable. Indeed, there is currently no known reason why devices cannot be written to and erased for an indefinite number of cycles, as long as breakdown (due to excessive applied voltage) of the chalcogenide or dielectric materials does not occur. In the case of the barrier devices, the write threshold remains high even after the barrier dielectric has been ruptured many millions of times as the erase process seems to "heal" the barrier, possibly by a localized anodic oxidation process.

1.3.8 High density solid-state memory

The key attributes of a high density solid state memory are (1) extremely low power/energy to avoid problems with power density/heating, (2) low voltage to allow the close packing of structures without breakdown and crosstalk, and (3) the ability for the devices to be scaled to

minimum lithographic dimensions. The memory described in this document would appear to meet these requirements and also adds the possibility of increased data density through multi-bit storage. To achieve high information storage density, the simplest layout is a cross point matrix where metal layer N forms the columns (e.g., bit lines) and metal layer N+1 forms the rows (word lines). The memory devices (cells) reside in vias at each crossing point. The main problem with this approach is that without some form of cell-to-cell isolation, parasitic paths may form through "rings" of on devices. Obviously, a diode or a transistor can be used for cell isolation purposes, as illustrated in Fig. 10. These components could be formed in the silicon substrate, along with all the other silicon components necessary for information control (decoders, sense amplifiers, etc.). However, to attain maximum storage density and free-up valuable silicon real estate, these elements should be fabricated using thin film techniques and reside in the same layers as the memory cells. This technology, usually based on amorphous or polycrystalline silicon, has existed for some time and is actually used extensively in TFT active matrix displays. The devices typically have a higher on resistance than the single crystal versions but this is largely immaterial in a system which uses low currents as the increase in voltage drop and power dissipation due to this effect will be minimal. The ultimate density could be attained by placing a thin film diode in each of the vias, in series with the memory elements, as shown in Fig. 11. In this way, it would be relatively simple to layer many levels of memory cells on top of each other to create a high density memory stack.

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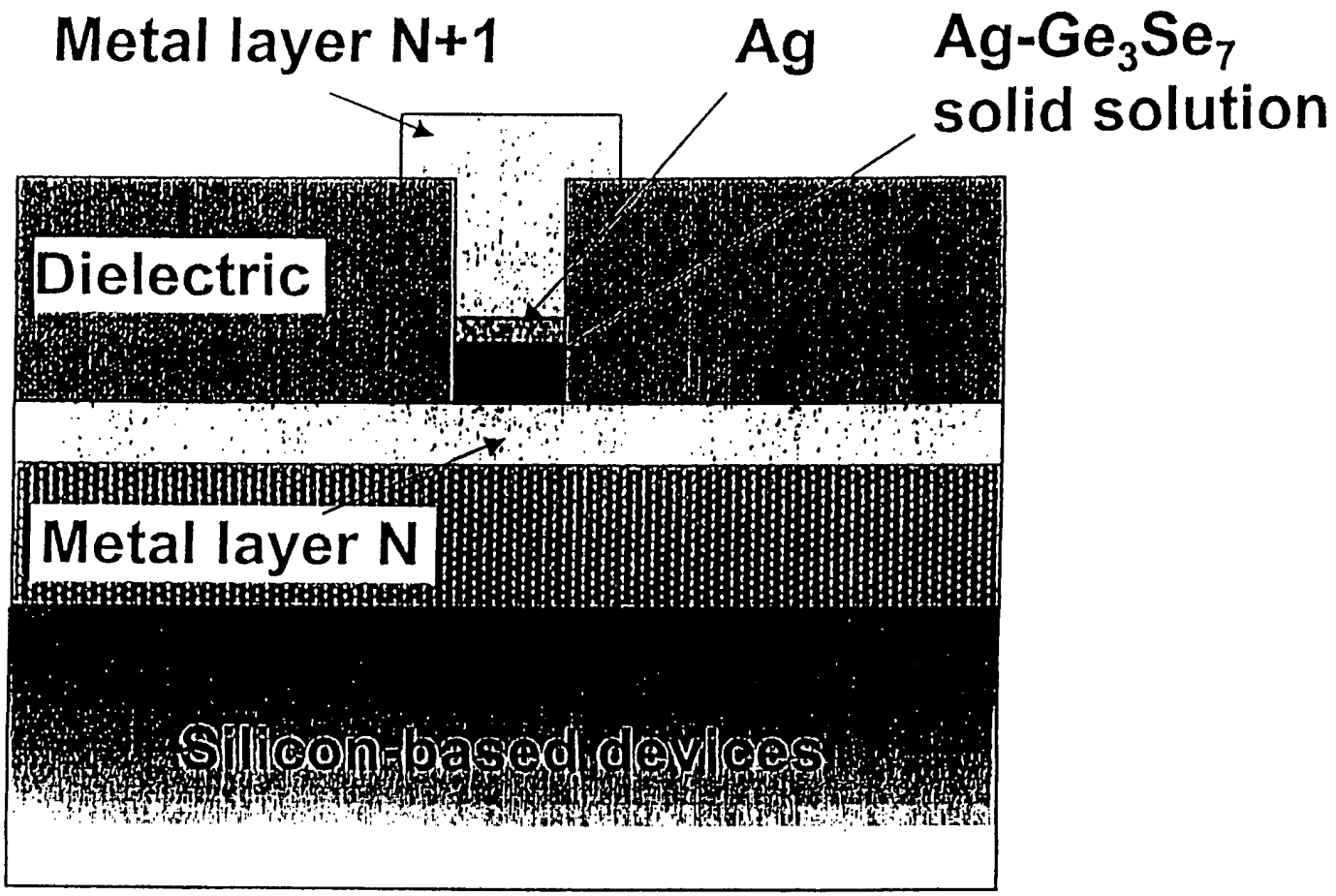


Fig. 1. Example of an "active in via" device cross section showing excess metal (Ag in this case) on the top surface of the solid solution.

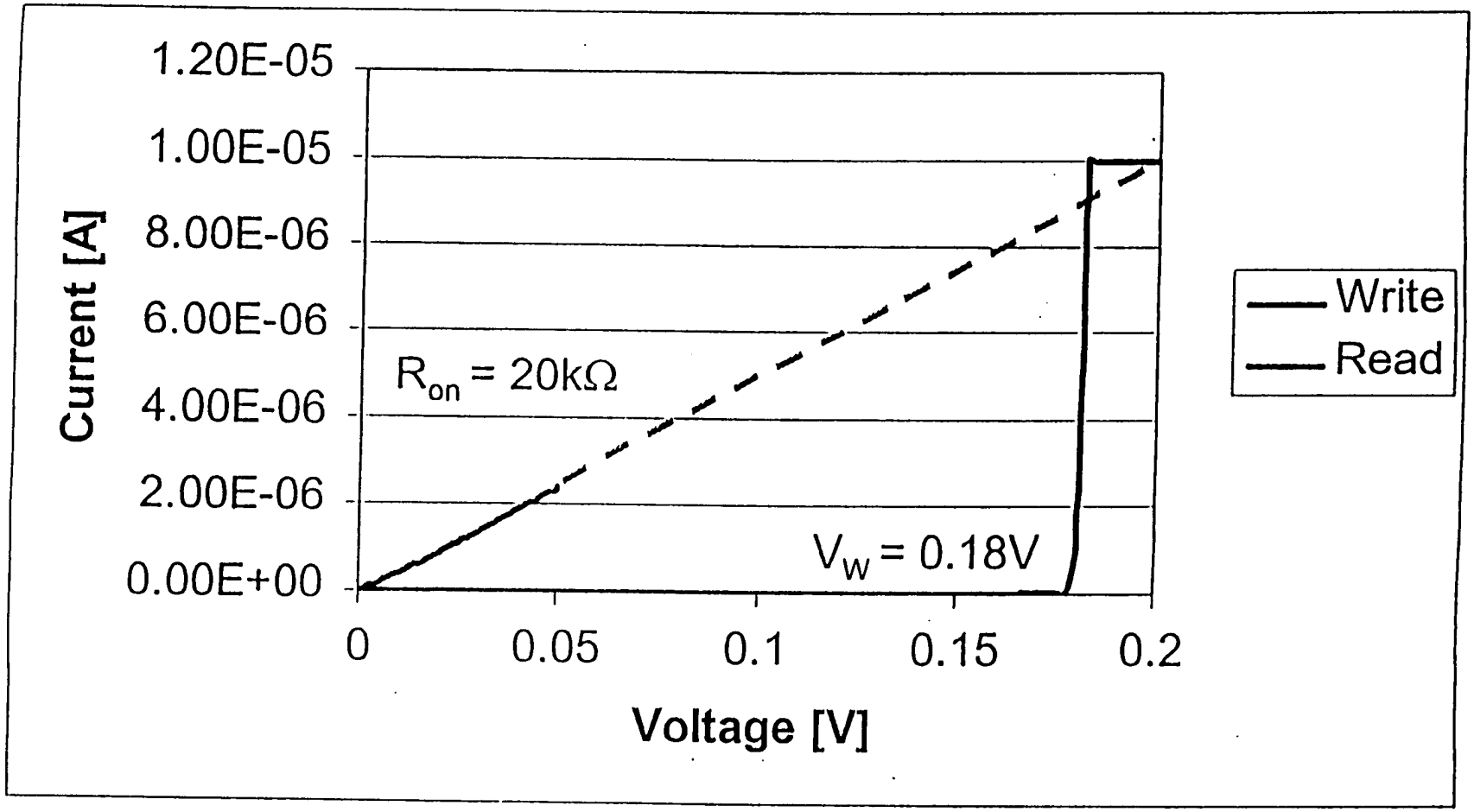


Fig. 2. Current-voltage characteristic of 0.8 μm test device with low write voltage (V_W) showing write and read voltage sweep operations.

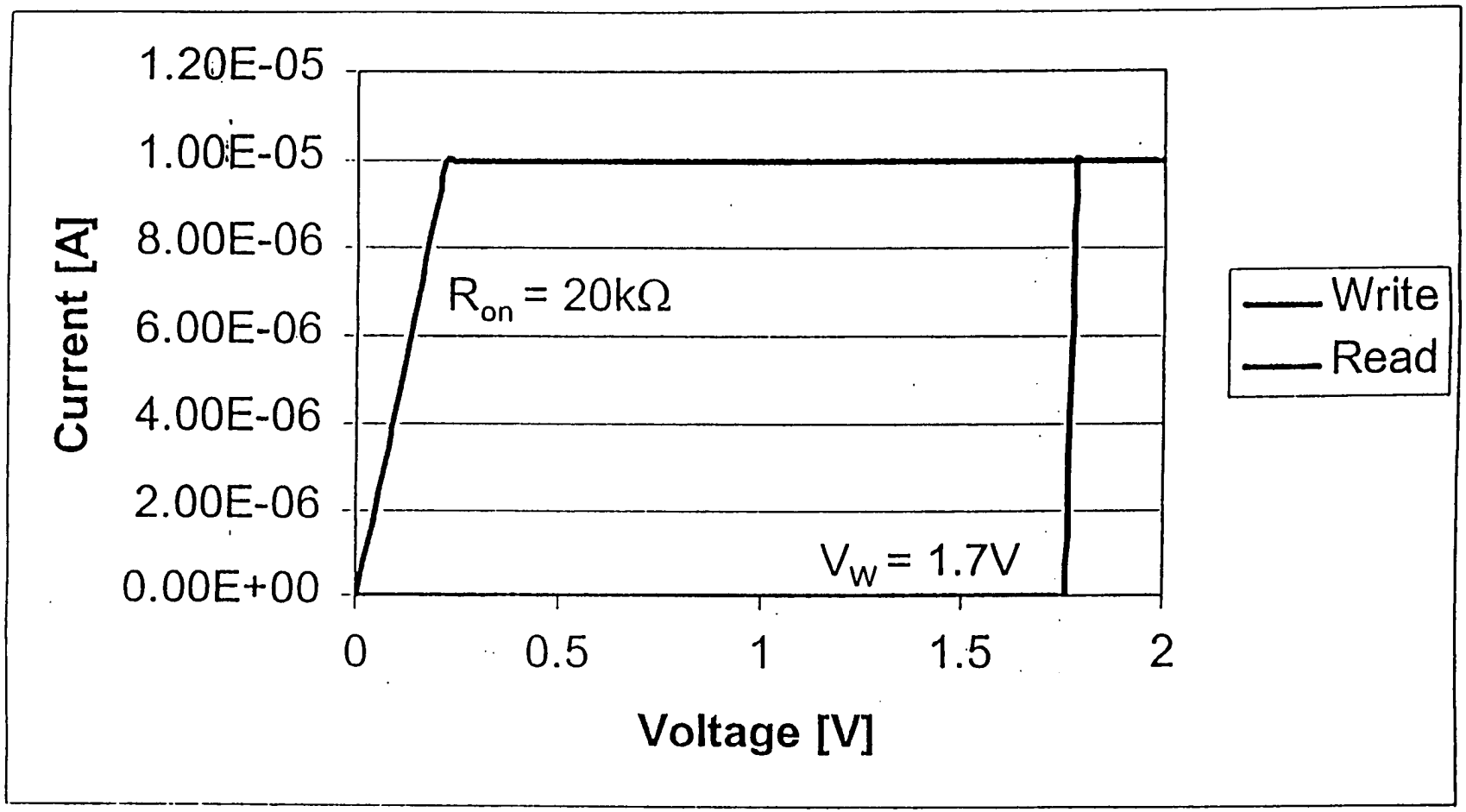


Fig. 3. Current-voltage characteristic of 4 μm test device with approximately 1.7 nm native oxide on anode showing write and read voltage sweep operations.

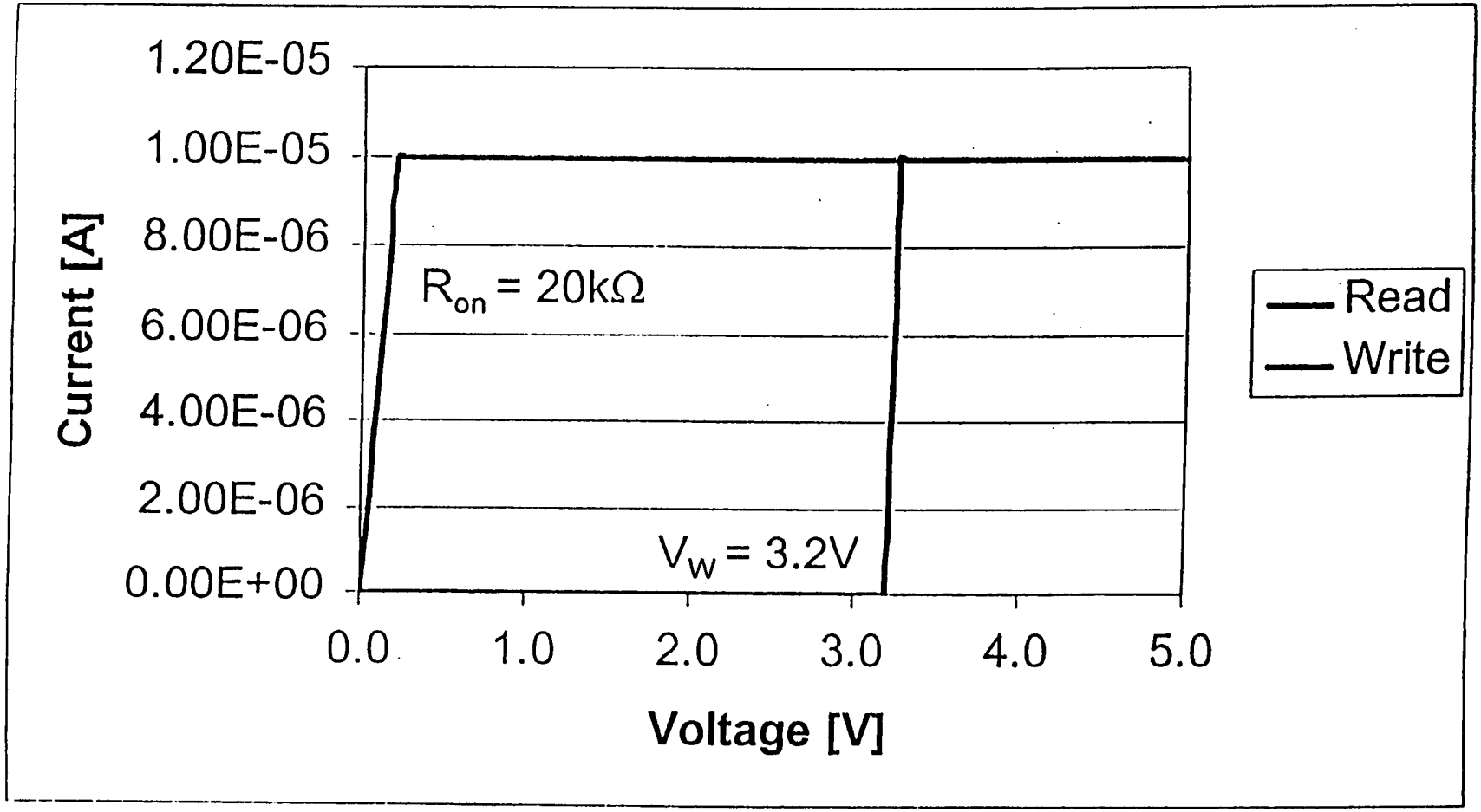


Fig. 4. Current-voltage characteristic of 4 μm test device with approximately 3 nm native oxide (effective thickness) on chromium anode showing write and read voltage sweep operations.

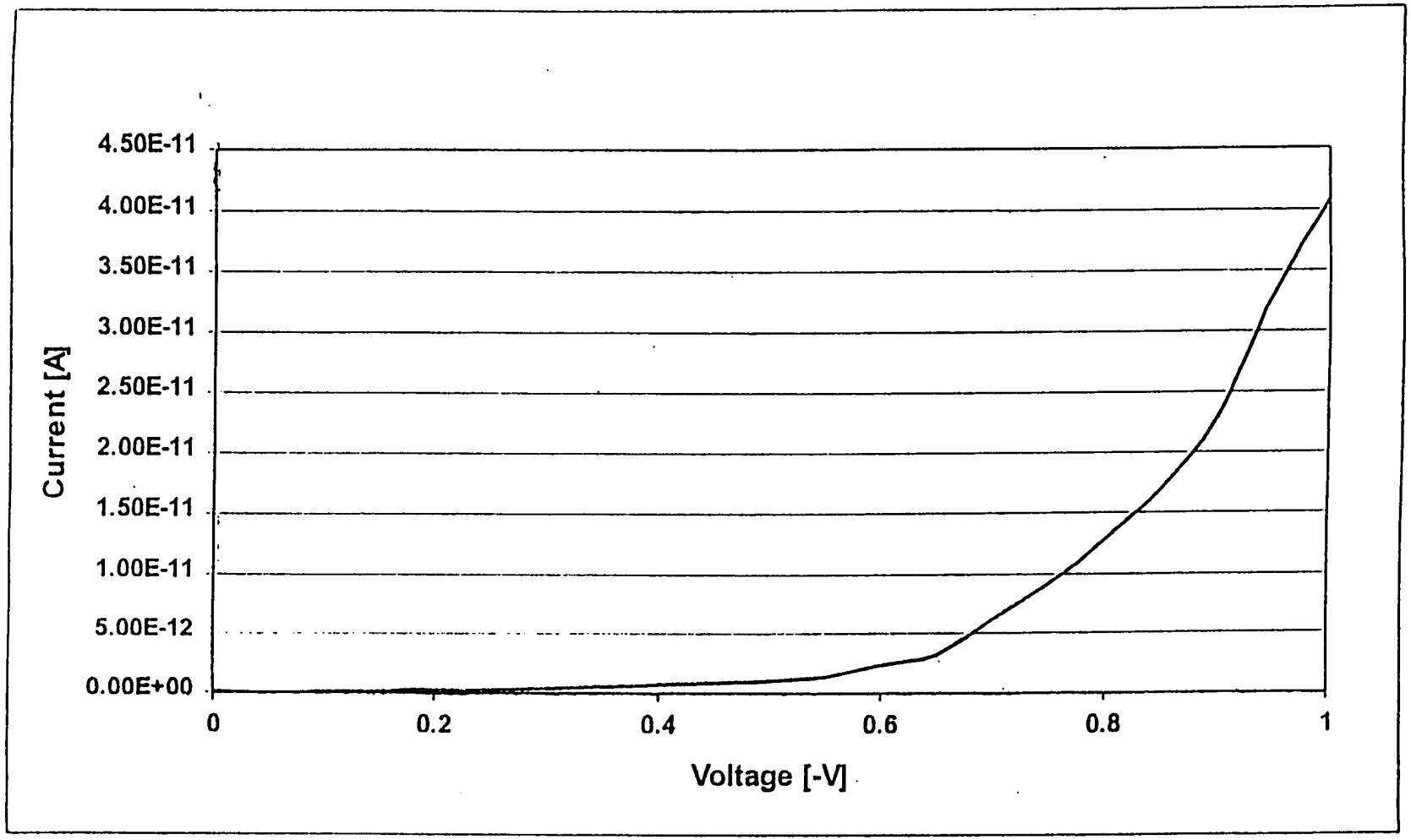


Fig. 5. Current-voltage characteristic of 4 μm test device with approximately 1.4 nm native oxide on anode in high resistance or "off" state.

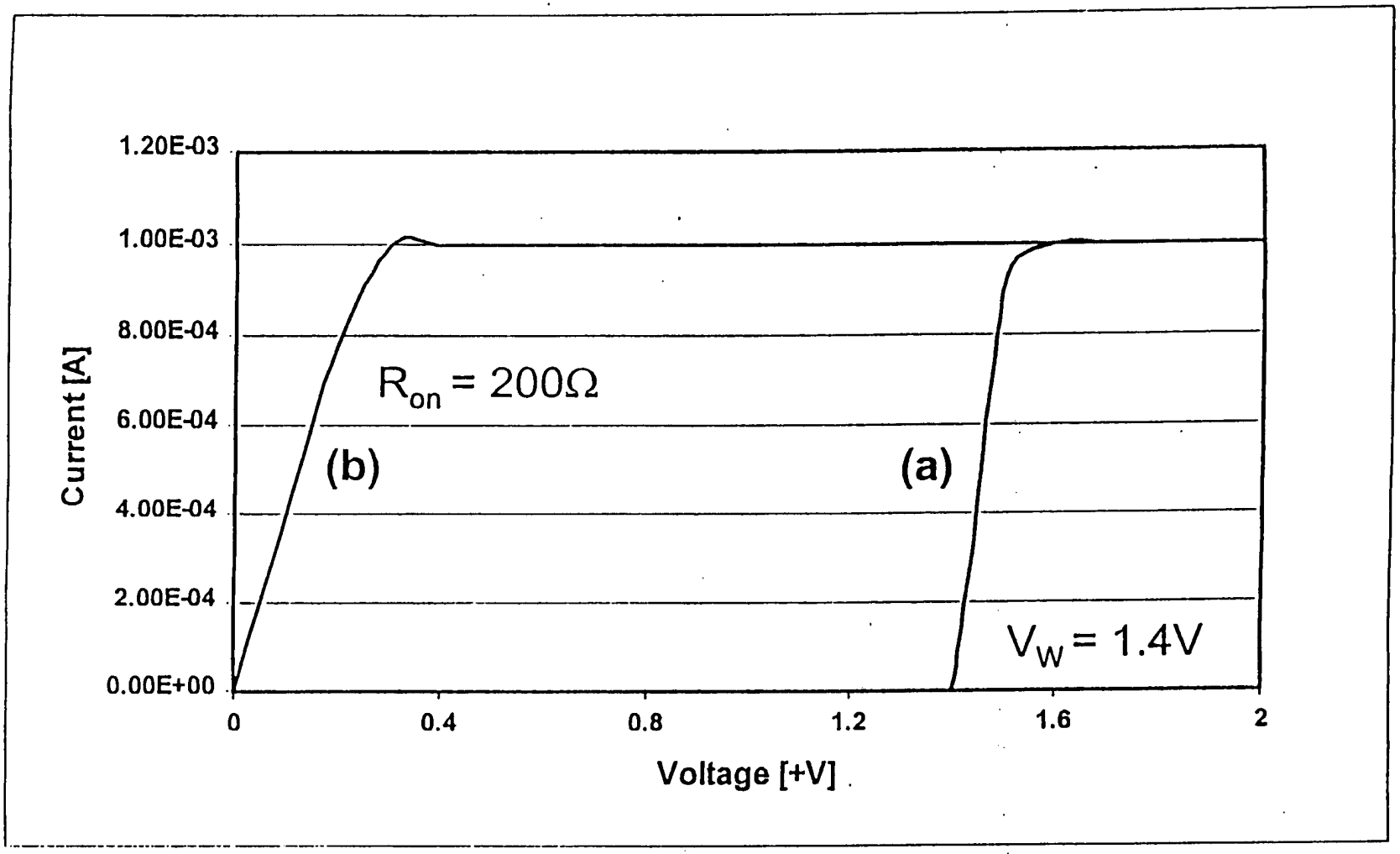


Fig. 6. Current-voltage characteristics of (a) device in the "off" state which switches to the "on" state at 1.4 V, (b) device in "on" state.

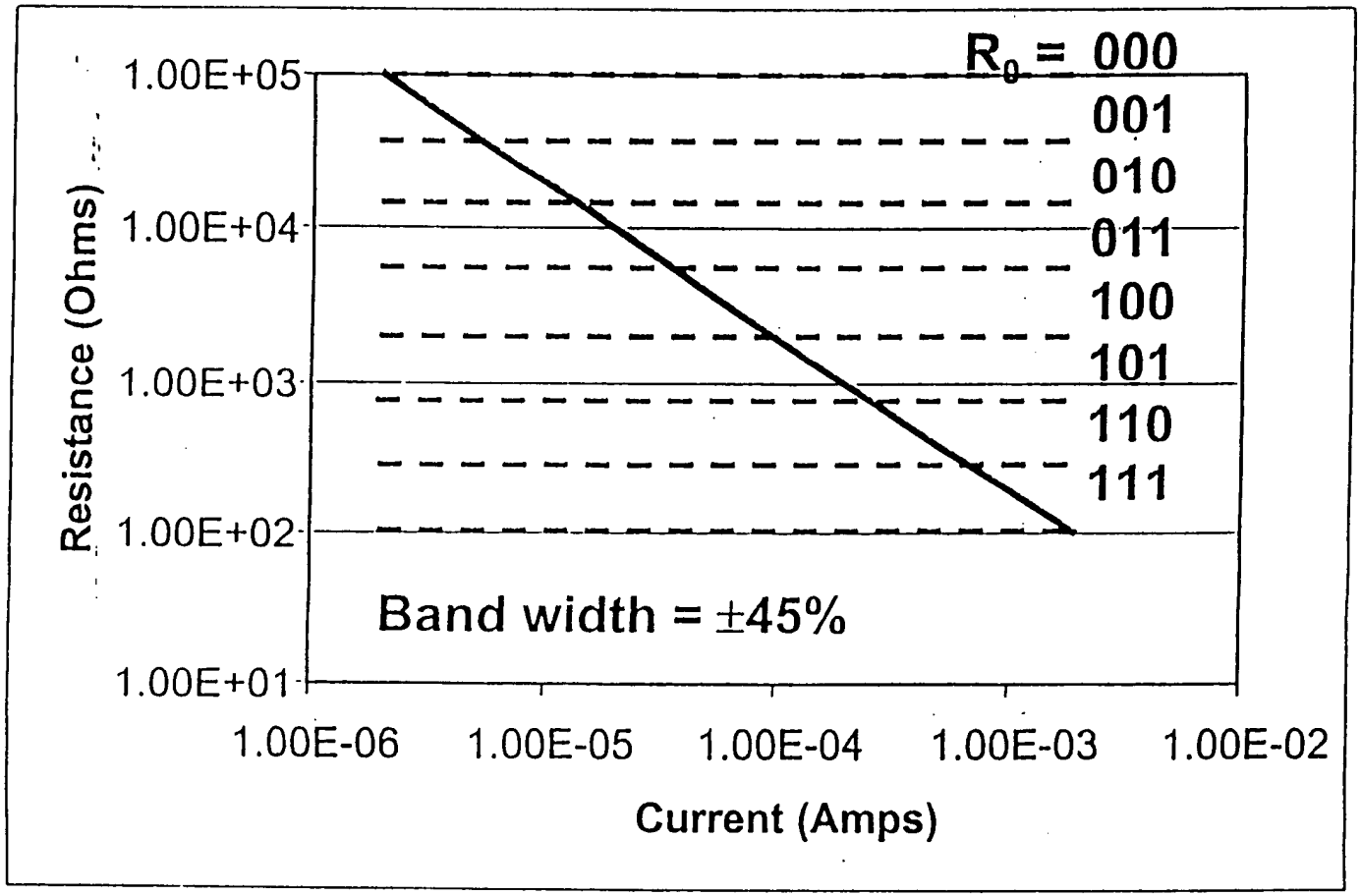


Fig. 7. Final device resistance as a function of programming current limit. Range has been split into seven "bands", each R_n±45% wide, where R_n is the mid range resistance value.

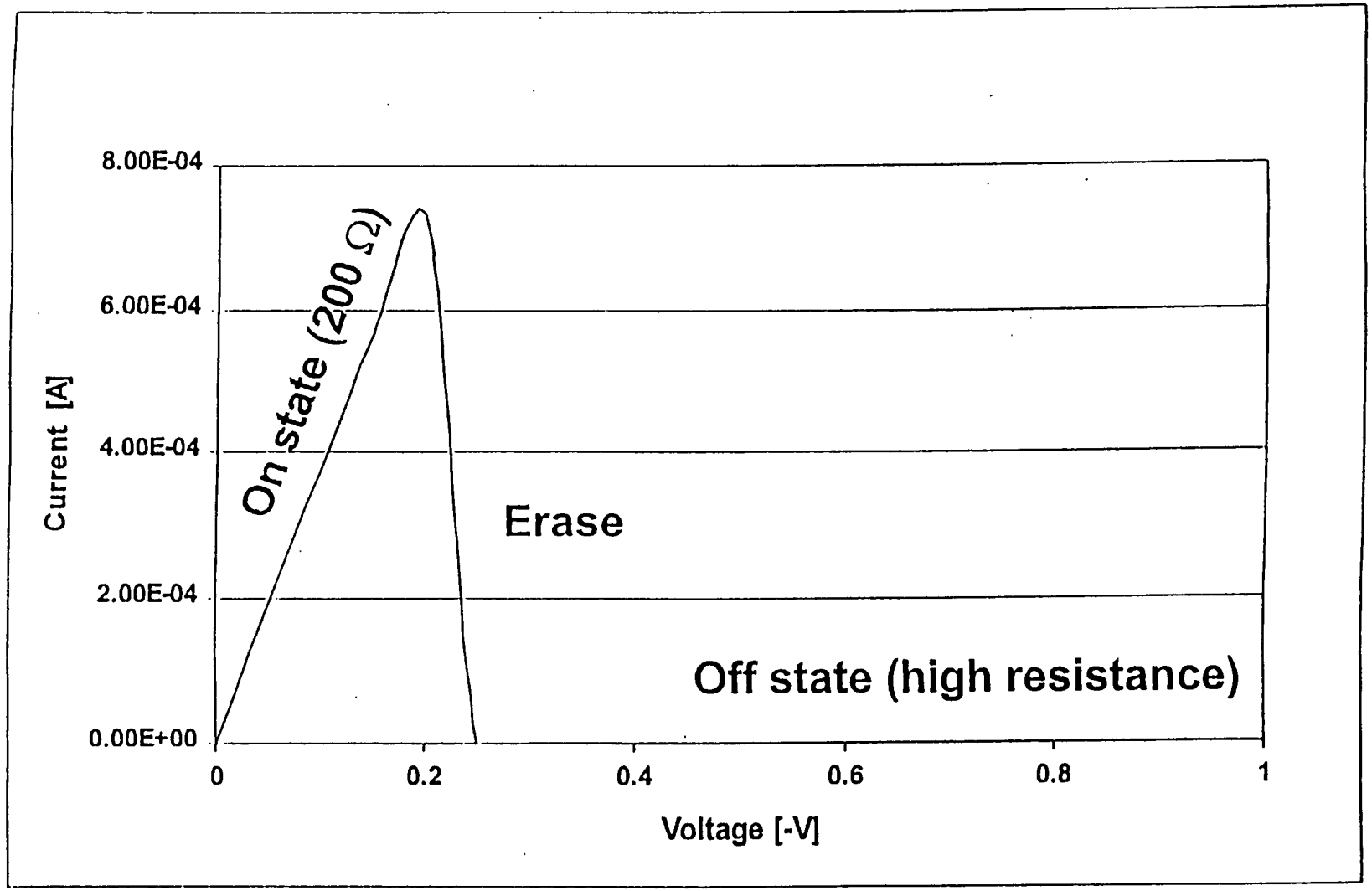


Fig. 8. Current-voltage characteristics of device in the "on" state which switches to the "off" state at 0.2 V.

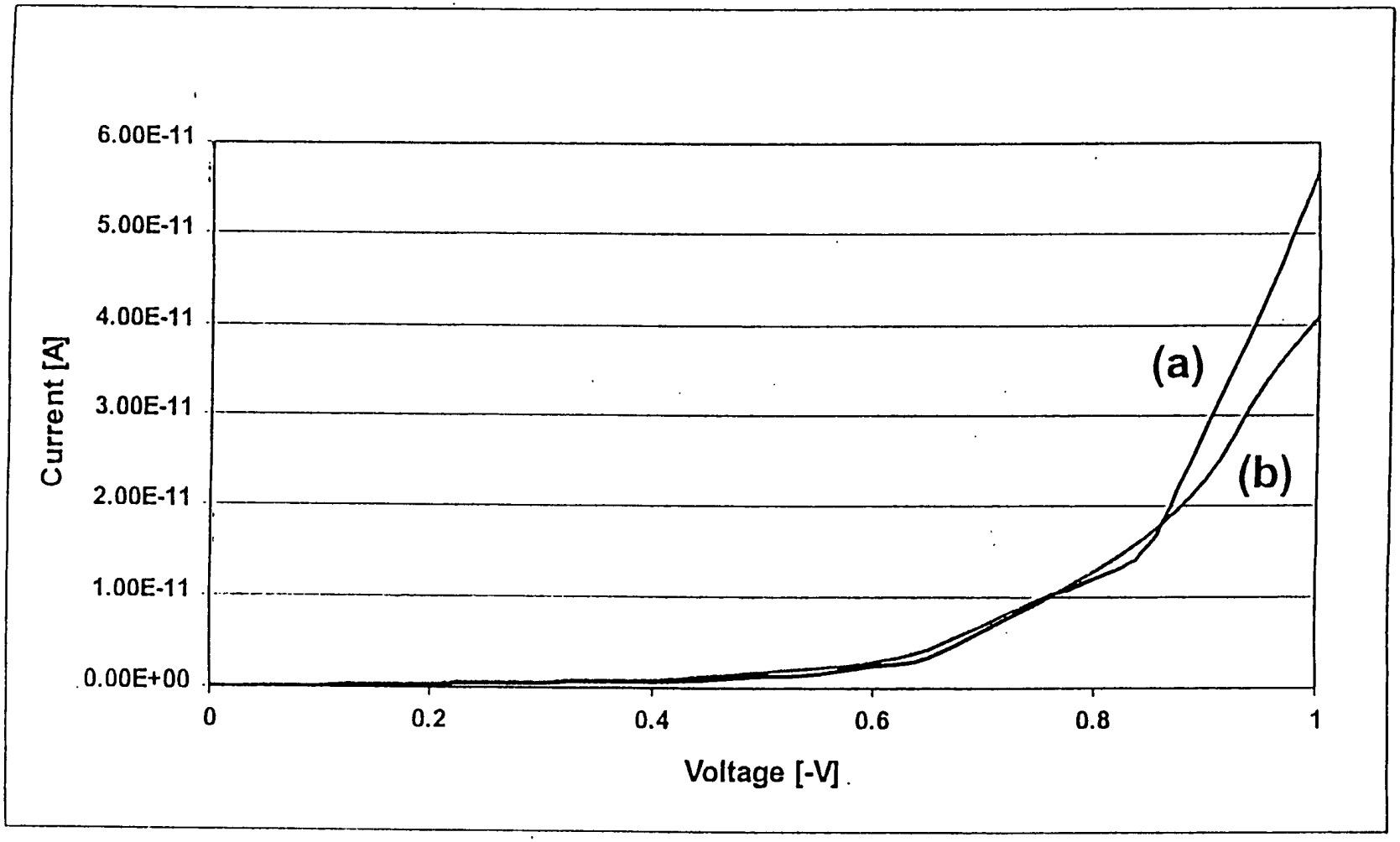
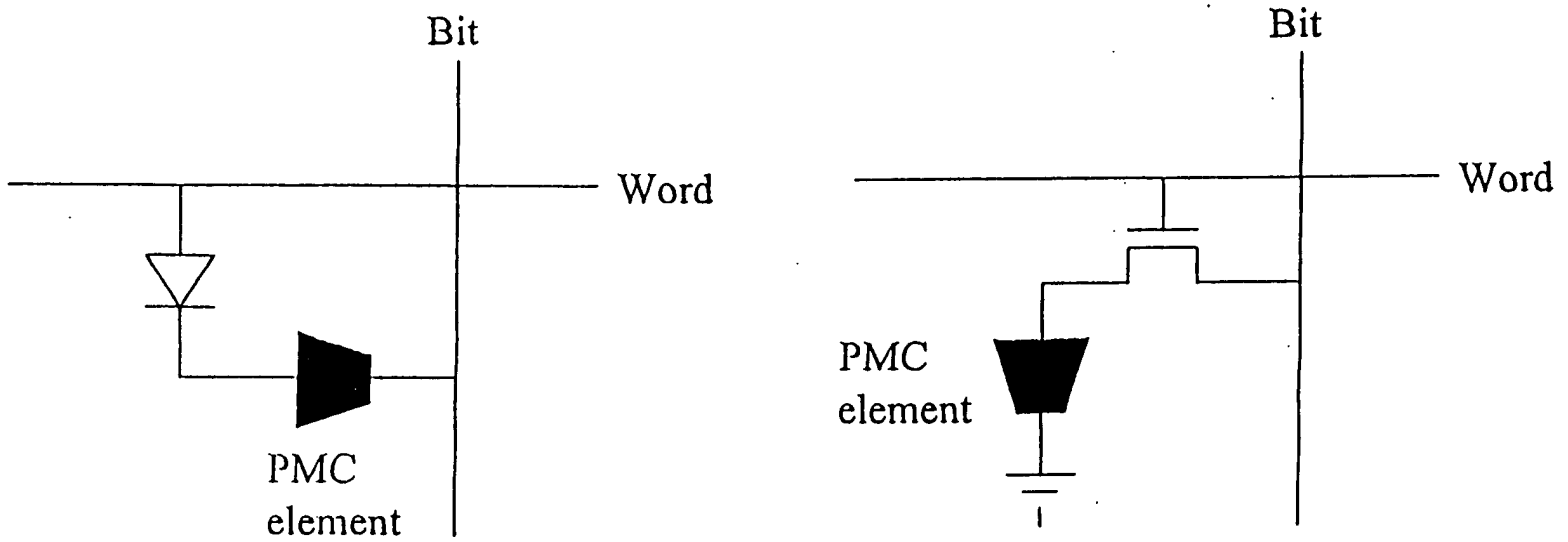


Fig. 9. Current-voltage characteristics of (a) erased device compared with (b) unwritten device. Both are in the high resistance state.



(a) Diode isolation

(b) Transistor isolation

Fig. 10. Example of memory cell isolation with (a) a diode and (b) a transistor.

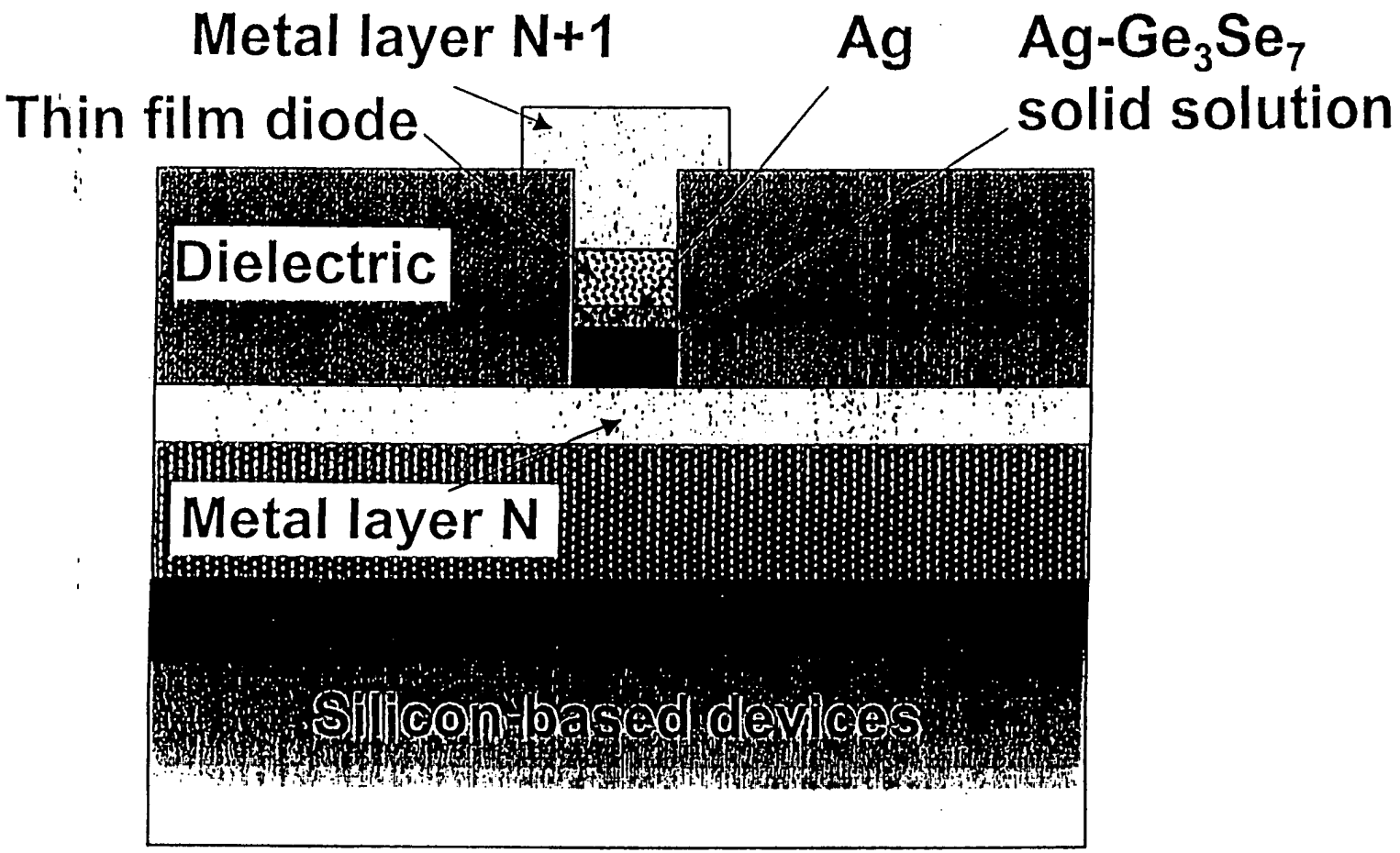


Fig. 11. Example of an "active in via" device with a thin film diode in the via in series with the memory element. Note that the diode could be placed above or below the solid solution.

Confidential

Michael N. Kozicki

Axon Technologies Corp.
and
Arizona State University

Presentation to
Micron Technology, Inc.
April 6, 2000

ASU *Center for Solid State Electronics Research*

AXON Technologies Corporatic

Solid Solutions

Chalcogenides are compounds of S, Se, Te (and O)

- As_2S_3, Ge_3Se_7, etc.

Metals (e.g. Ag, Cu) can be dissolved in chalcogenide glass to form a solid solution

- introduced by thermal diffusion or photodissolution (uv)

Example - Ag in Ge_3Se_7

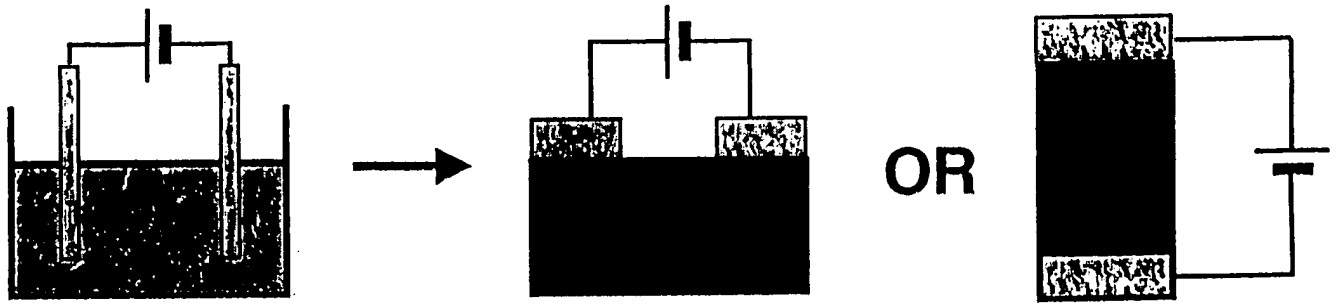
- $Ge_3Se_7 = 3GeSe_2 + Se$ ($GeSe_2$ glass has SiO_2–like structure)
- Ag reacts with excess Se (Ag_2Se) and acts as a network modifier - up to 32 at.% Ag possible
- Ag in solution $\rightarrow Ag^+$ and moves with field ($\mu = 10^{-5} - 10^{-4}$ $cm^2/V.s$?)

Transport number is high

- poor electronic conductors
- solution resistivity is therefore high (hundreds of Ω.cm)

Electrochemistry

Solid solutions are not unlike liquid electrolytes!



- Cathode (conductor): $M^+ + e^- \rightarrow M$ *electrodeposition*
- Anode (with excess M): $M \rightarrow M^+ + e^-$ *electrodissolution*

Redox reaction proceeds at low voltage

- approximately 0.18 V threshold
- maintains M^+ concentration in solution
- ions move through solution by a "coordinated motion"

Which Material?

We started with As_2S_3 and AsS_2 but ...

Arsenic compounds pose technological challenges

- toxicity
- Ag precipitation
- As outdiffusion and sublimation
- low glass transition temperature

AsS_2 - 145ºC	As_2S_3 - 184ºC
$AsSe_2$ - 131ºC	As_2Se_3 - 173ºC

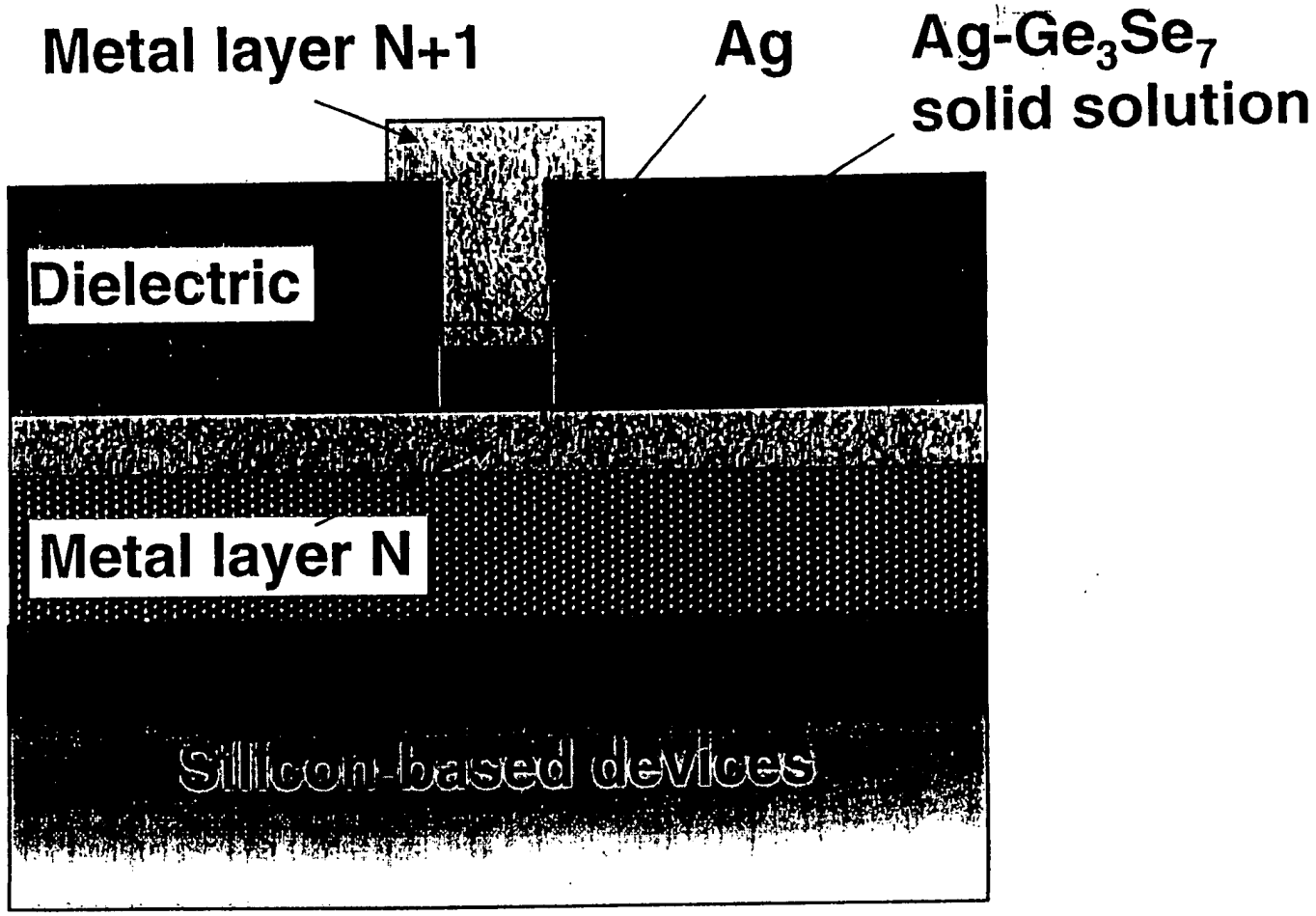
- Germanium compounds are better ...
  - better glass transition temperature

GeS_2 - 500ºC	Ge_3S_7 - 450ºC
$GeSe_2$ - 425ºC	Ge_3Se_7 - 400ºC

On the other hand, tellurides stink!

- weak bonding and unstable glasses
- crystallizes very easily at low T (even at resist hard bake)
- Te is very toxic

Example of an "Active in Via" Device



Electrical Characteristics: "Off State"

Solution resistance is high

- 100s $k\Omega.\mu m^2$ in a 30 nm long structure

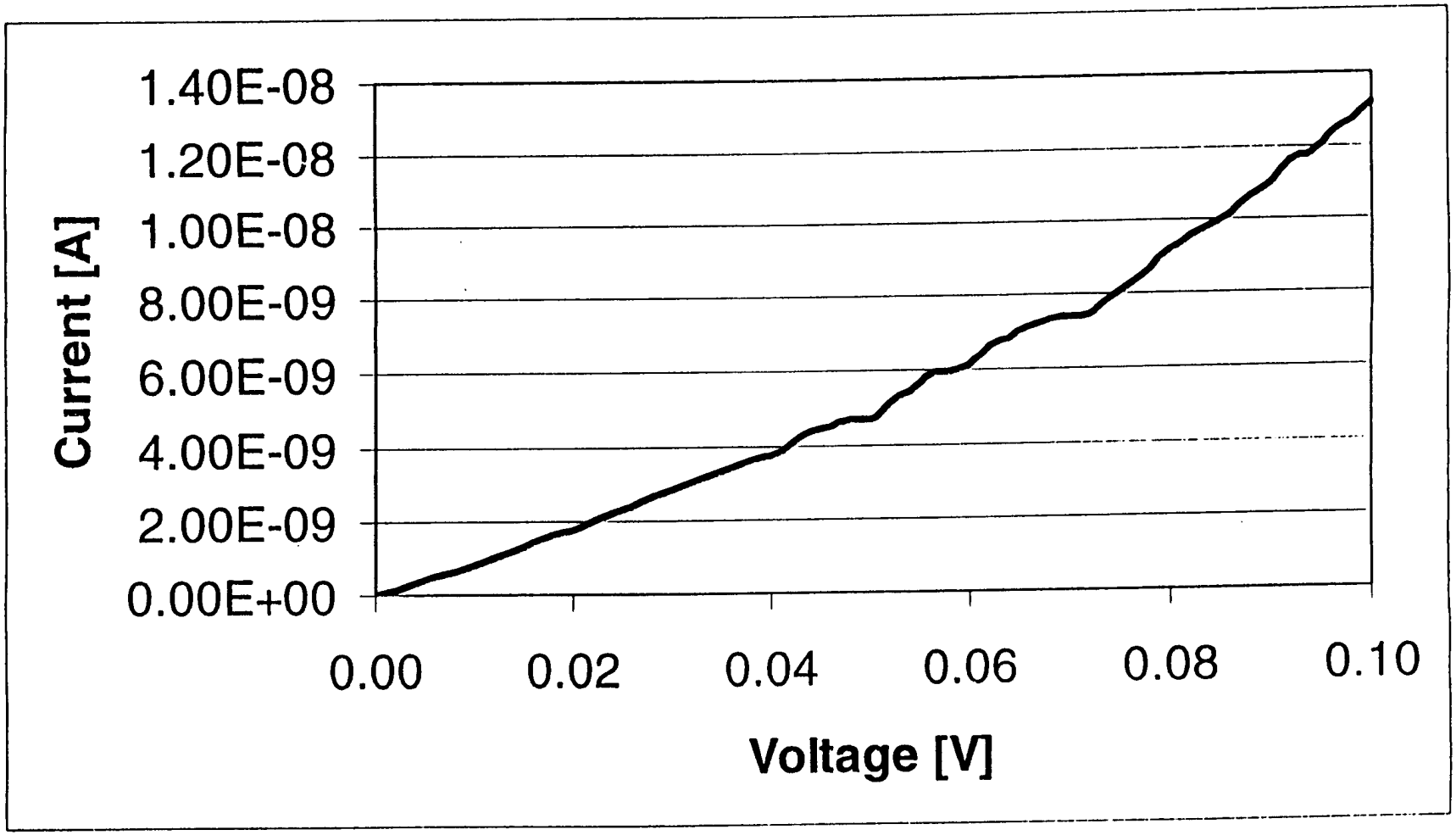
Double layer at metal-solid solution interface leads to capacitive character

- capacitance in the order of 10 $fF/\mu m^2$
- current flow is Schottky barrier-like, $I \sim e^{qV/kT}$
- adds high small signal resistance (5 $M\Omega.\mu m^2$ @ 0.1V)

Additional tunneling barrier at cathode greatly increases resistance

- can increase overall resistance to tens of $G\Omega.\mu m^2$

Characteristics of 0.8 μm device with Ni cathode in off-state subthreshold region



Electrical Characteristics "On State"

- Applied voltage above electrodeposition threshold results in growth of silver "wire" from cathode to anode
  - on surface of solution at interface with dielectric
- Electrodeposit growth shorts-out solution and double layer
  - greatly reduced resistance
  - purely metallic character
- Resistance of on state depends on amount of charge applied during electrodeposition

Charge Requirements

Sample calculation assumptions:

- Electrodeposition is 100% efficient - total charge required per cm^3 of Ag electrodeposit = 9.28×10^3 C
- Electrodeposit has uniform cross section
- Ag thin film resistivity is 100× the bulk value

For a 30 nm long connection with a resistance of 1 kΩ, electrodeposit volume is 1.35×10^{-18} cm^3.

Charge required is 1.25×10^{-15} C

Energy required is 0.25 fJ!

A constant applied current of 1 μA would allow switching in the nsec regime

- But high off resistance limits current!
- What are the other limiting factors?
- What about parasitics/double layer capacitance?

Speed Predictions

Growing electrodeposit becomes the cathode - high field at tip leads to preferential deposition

Moving tip "harvests" ions from solution as it progresses and tip field increases

Electrodeposit is typically very thin - around a nm thick (x 10s of nm wide)

Solution contains many tens at. % of metal and so it takes only a few nm of depth to supply growth

Ions only have to move a few nm in high field

If field is in the order of 10^6 V/cm and mobility is 10^{-4} $cm^2/V.s$, ion velocity will be 1 nm/nsec

The ions therefore take only a few nsec to come out of solution

Self-Limiting On Resistance

If a constant current I_{const} is applied, the voltage across the device will depend on its resistance R by $V = I_{const}R$

Electrodeposition will occur as long as the voltage is above the threshold (0.18 V)

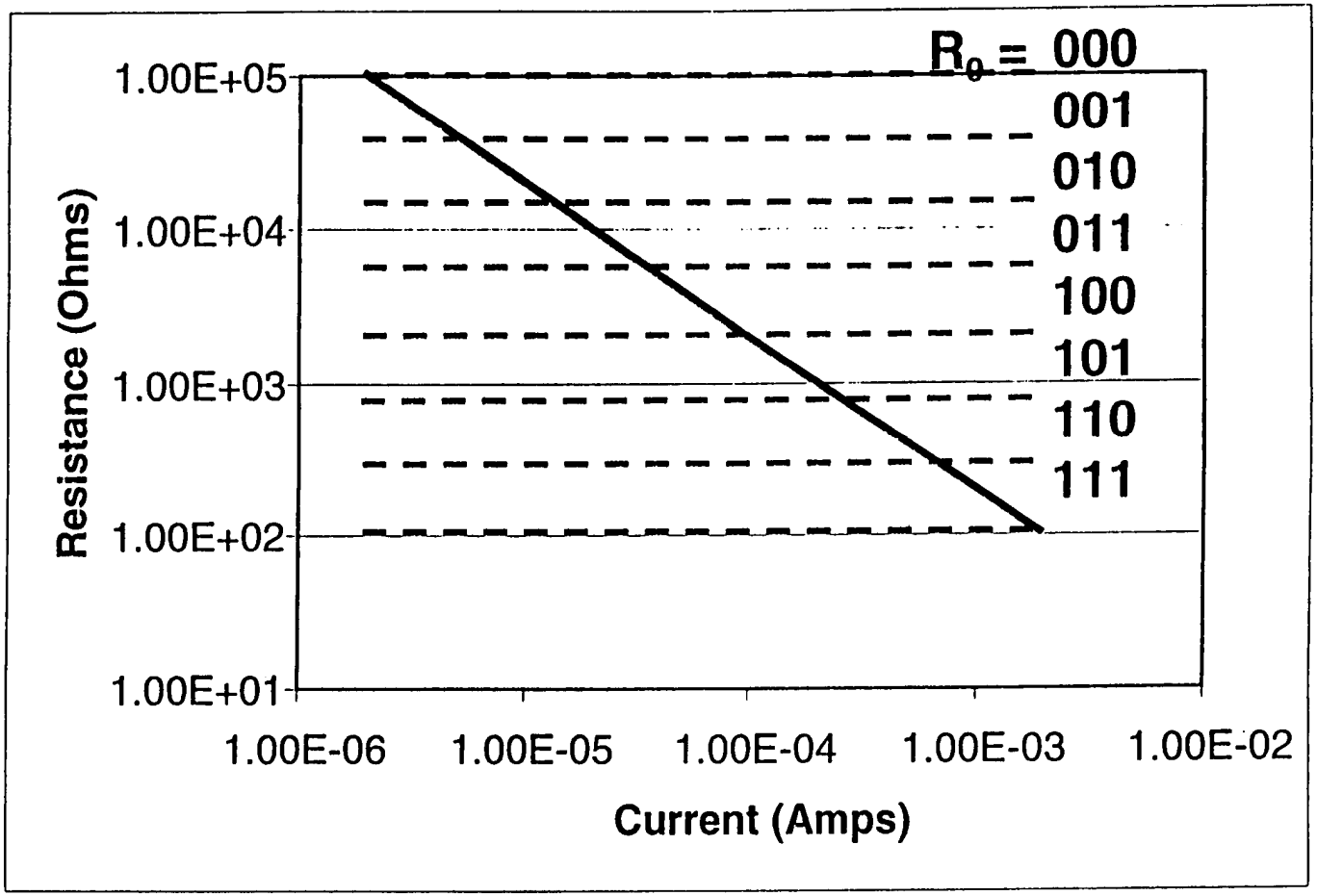
When the electrodeposit connection is formed, the resistance will drop and so will the voltage

The final resistance R_{on} of the device is therefore determined by the expression

$$R_{on} = 0.18/I_{const}$$

This leads to a programmable self-limiting on resistance

Multi-Bit Programming Scheme?



Range has been split into seven "bands", each ±45% (from each midpoint) wide

Importance of Asymmetry

Redox reaction will only proceed if the cathode can supply electrons and the anode can supply ions

A device which has an "indifferent" cathode and excess metal at the anode can only form an electrodeposit in "forward bias"

Once formed, electrodeposit is erased by applying a "reverse bias" above -0.18 V

- redox reaction occurs in reverse
- electrodeposit is now the anode and dissolves back into solution
- electrodeposition occurs at the cathode (original anode) at the point where electrodissolution originally occurred

Control of Write Threshold

Electrodeposition threshold is set by redox reaction - fundamental write/erase limit

Write threshold may be significantly increased by placing a tunneling barrier on the cathode

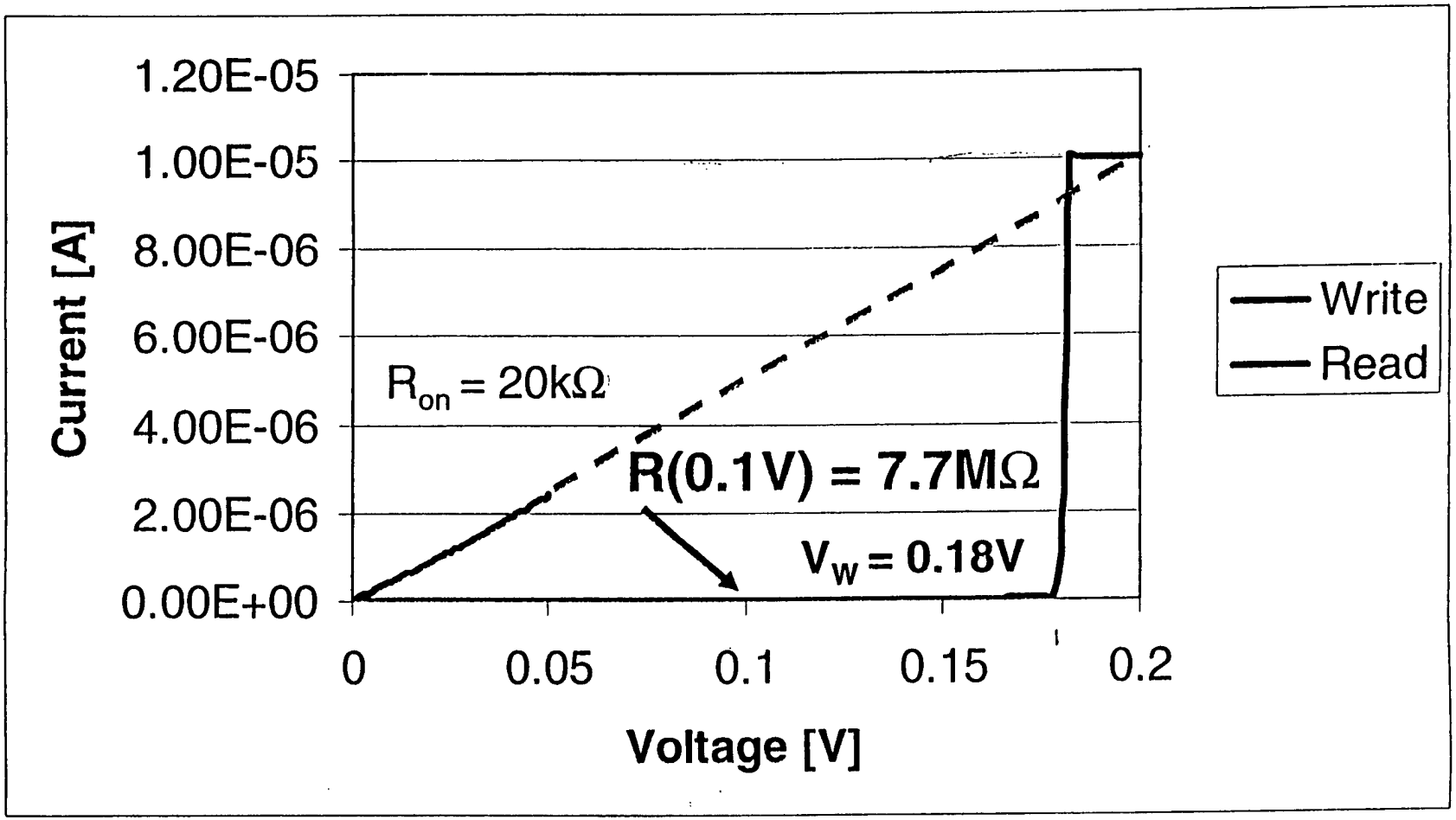
Electrodeposition occurs on this barrier as electrons can tunnel through to solution

Connection from cathode to anode is not complete until barrier is broken down

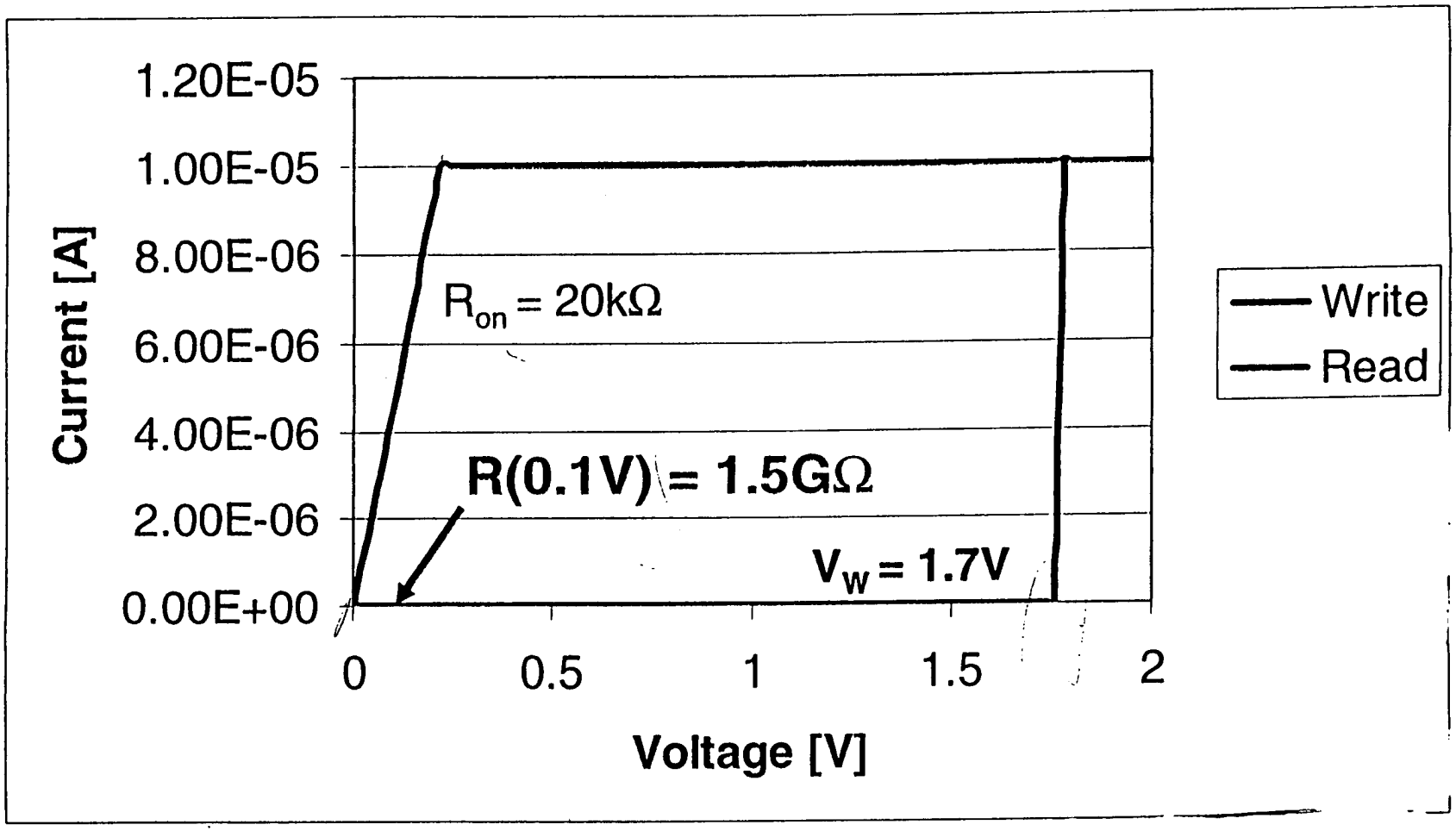
This occurs when applied voltage reaches V_b for the barrier - typically 1V/nm of thickness

Barrier is "healed" during erase by anodic oxidation(?)

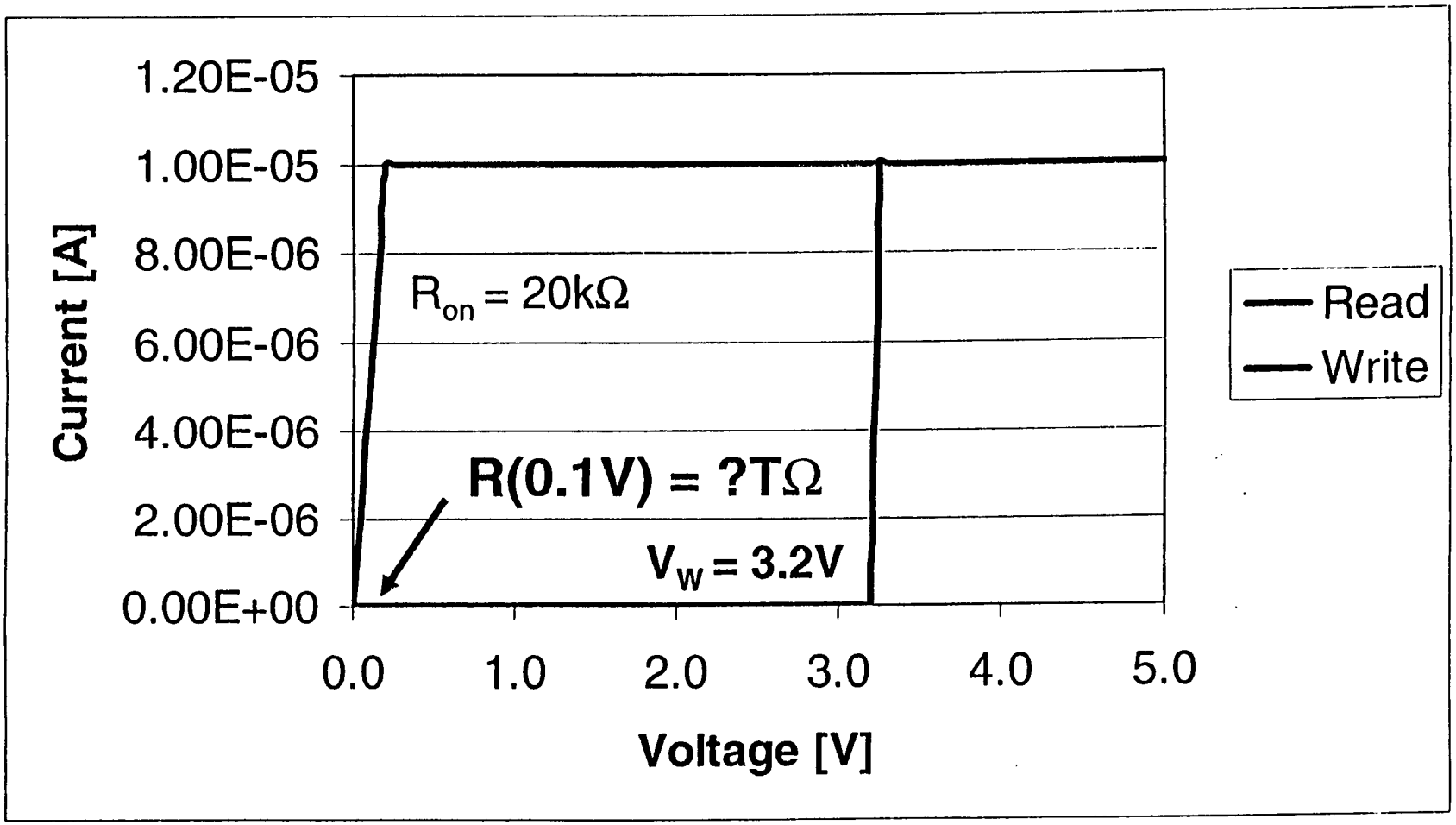
Characteristics of 0.8 μm test device with low write voltage (V_W)



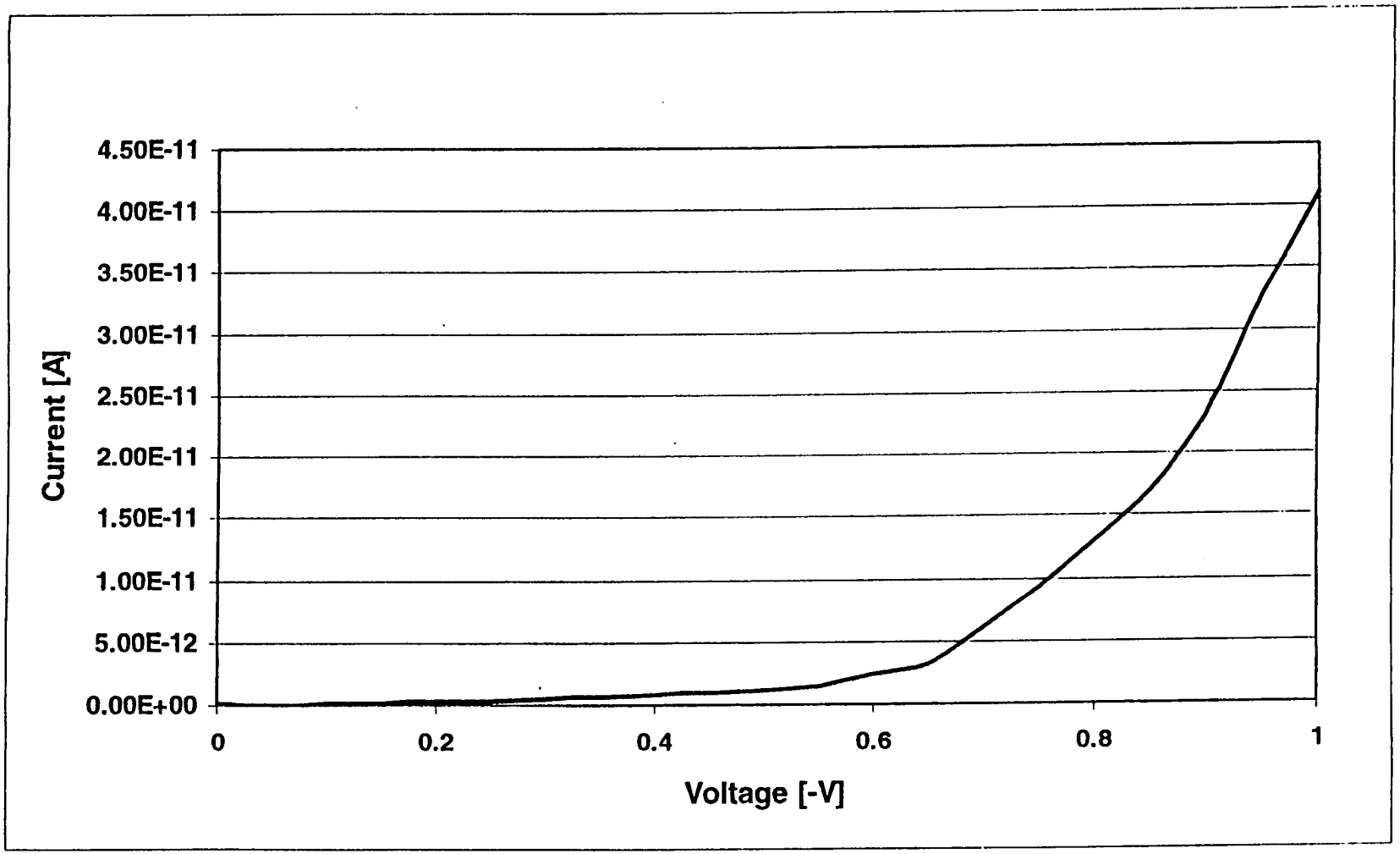
Characteristics of 4 μm test device with approximately 1.7 nm oxide on cathode



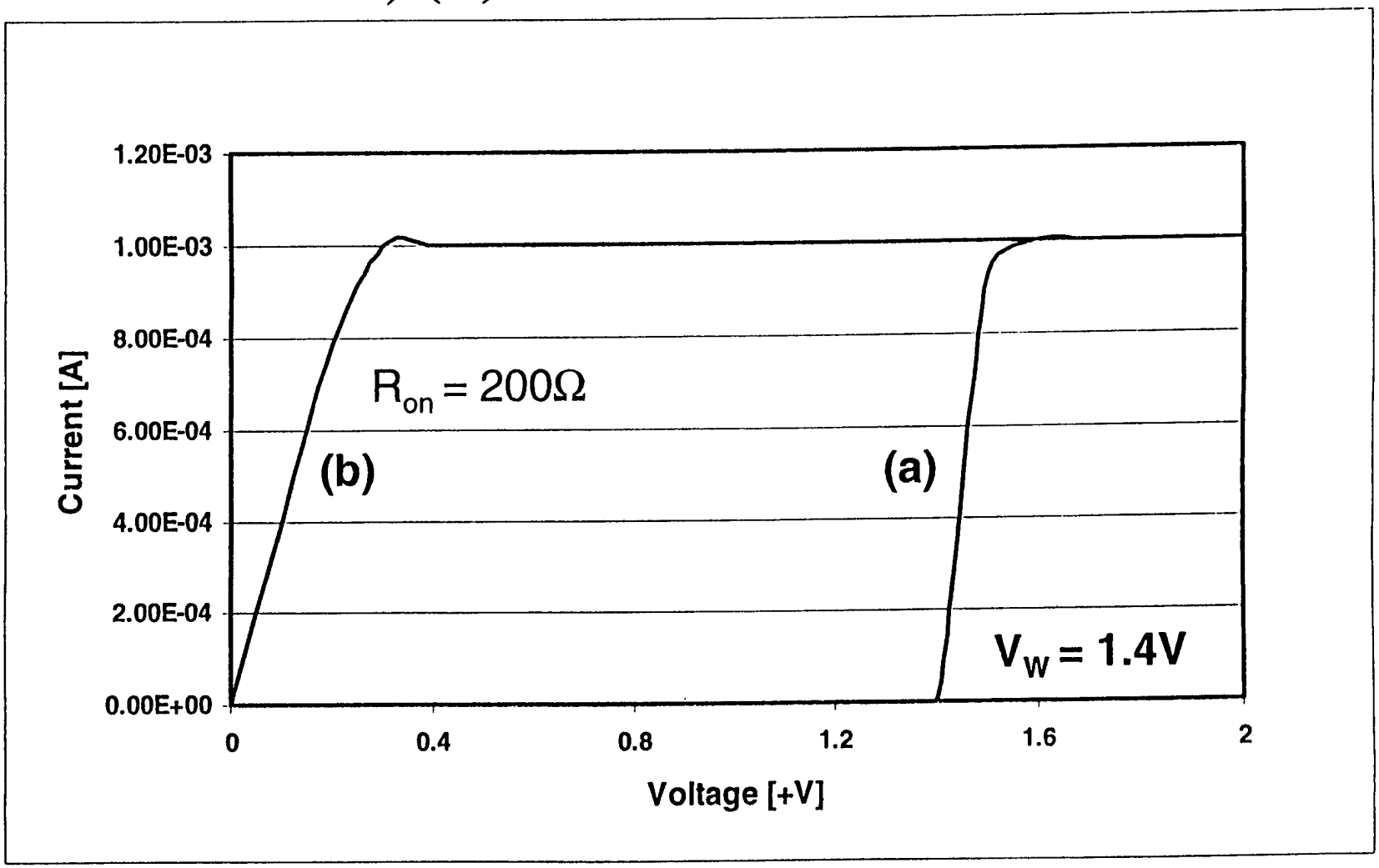
Characteristic of 4 μm test device with approximately 3 nm oxide on cathode



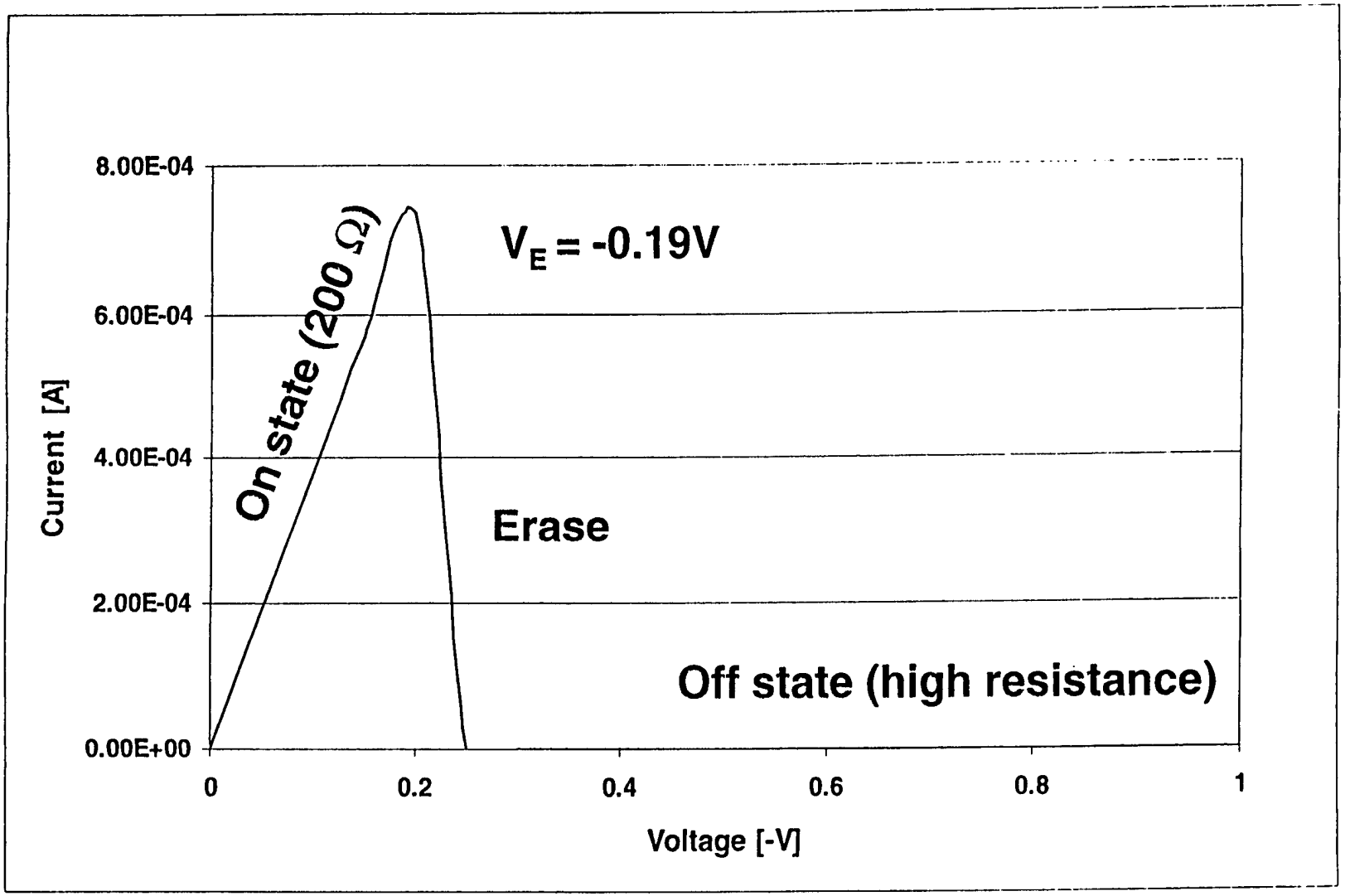
Characteristics of 4 μm device with approximately 1.4 nm native oxide on cathode in "off" state



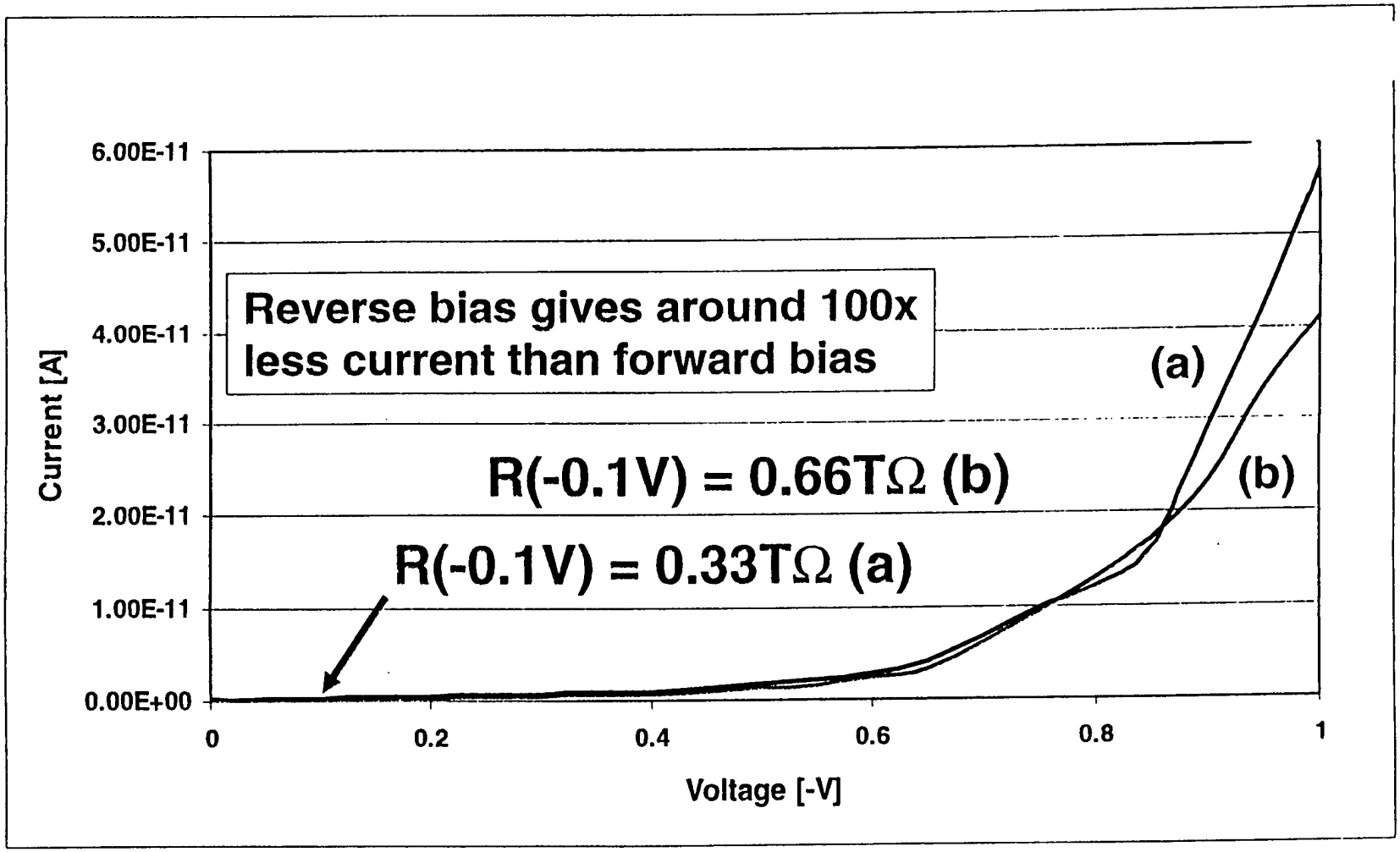
Characteristics of (a) device in the "off" state which switches to the "on" state at 1 4 V, (b) device in "on" state



Characteristics of device in the "on" state which switches to the "off" state around -0 2 V



Characteristics of (a) erased device compared with (b) unwritten device



Endurance and Retention

- **Electrodeposition/electrodissolution cycle should be repeatable indefinitely in the absence of significant material changes**
  - we have been able to demonstrate 10^7 to 10^8 cycles but
  - many devices fail in on-state after a few 1000 cycles
  - stuck bit is due to breakdown of surrounding dielectric
- **Electrodeposit on "saturated" solid solution should be stable indefinitely**
  - we have been able to show zero percent resistance change over several hours
  - measurement is affected by probe resistance changes
  - devices are highly sensitive and are susceptible to noise and discharge events

Read Strategies

Devices are highly sensitive - presents problems for non-disturb read

Possible read options are:

- destructive - deliberately write or erase cell to detect state
- low voltage (sub-threshold) - <0.18 V forward or reverse
- short pulse (forward bias) to charge double layer only
  - » C_{dl} will be a fraction of a fF in a small geometry device
  - » A10 nsec pulse at 10 nA will charge this
  - » Charging current is "non-Faradaic" - no electrodeposition

Non-destructive options essentially utilize current control or charge limiting

Issues

- Materials deposition/device fabrication
  - deposition methods
  - electrode materials
  - barrier materials
  - glass transition temperature
- Thermal stability
  - during processing
  - operation
- Materials and device performance
  - write, read, erase energy
  - retention, endurance
  - failure mechanisms
- Etc.?!!

Short Term Work at ASU

- **Build glass synthesis facility**
  - existing facility is inadequate
  - new facility will be in CSSER with controlled access
  - may use existing facility at U. Cincinnati to avoid delay
- **Synthesize source material for evaporation**
  - $GeSe_2$ as well as Ge rich and Se rich glasses
  - GeS_2 as well as Ge rich and S rich glasses
  - perform analysis
- **Fabricate basic test structures**
  - determine gross material properties
- **Continue to compile materials database**
  - information is sparse and scattered

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September 5, 2000

By certified mail
Return receipt requested

Mr. Mark Durcan
Micron Technology, Inc.
8000 S. Federal Way, MS 840
Boise, Idaho 83716-9632

RE: Invention Disclosures (ASU Case Nos)

M1-006	"Solid Solution for the Programmable Metallization Cell"
M1-007	"Optimized Electrodes for the Programmable Metallization Cell"
M1-008	"Programmable Metallization Cell With Floating Electrode"
M1-009	Method for the Synthesis of Macrohomogeneous Germanium Chalcogenide Glasses"
M1-010	"Common Electrode Configurations for the Programmable Metallization Cell"
M1-011	"Ultra Low Energy Programmable Metallization Cell Devices"

Dear Mark,

I have received notification from ASU of the above-referenced invention disclosures. In the opinion of ASU, all the disclosures represent "IMPROVEMENT INVENTIONS" as defined in the Research Agreement between Axon and ASU. I have therefore instructed our patent counsel to prepare, file, prosecute and maintain patents on these disclosures.

This letter is written in compliance of with Paragraph 3.2 of the Research and License Agreement dated March 22, 2000 between Micron Technology, Inc. and Axon Technologies Corporation. The text of each of the referenced disclosures is included with this letter.

Sincerely,

Vic Lyn
Executive Vice President

Cc: Roderic Lewis, General Counsel, Micron Technology, Inc.
Michael Kozicki, ASU
Quinn Williams, Snell & Wilmer
Cindy Pillote, Snell & Wilmer

Enclosures

ASU ARIZONA STATE UNIVERSITY

AUG 2000
Technology Collaboration And Licensing

CONFIDENTIAL

DISCLOSURE AND RECORD OF INVENTION FORM

Once completed, this form is considered proprietary & confidential by the Arizona B ard f Regents.

Arizona State University
Office of Technology Collaborations & Licensing

ASU Disclosure # M1-008

1. **Short descriptive title of the invention.**

PROGRAMMABLE METALLIZATION CELL WITH FLOATING ELECTRODE

CIRCUMSTANCES OF THE INVENTION

2. **List the funding source(s) for the project under which this invention was made. Identify by contract or grant number as well as Area/Org No. and name of the Principal Investigator.**

Funding Source/Sponsor	Contract/Grant Number	Area/Org No.	Principal Investigator
AXON TECHNOLOGIES	TCL 00-1048	DWT 0099	M.N. KOZICKI

3. **For any "Inventor" named on page 3 who is not employed full-time by Arizona State University, please identify their employers, the percent of salary time funded by such other employer, the nature of the other employment (such as research, teaching or clinical duties), AND WHERE THEIR INVENTIVE CONTRIBUTION WAS MADE.**

4. **When did you first conceive this invention?**

5. **What is the date of the first written record (notebook, letter, proposal, drawing, etc.) of this invention? Identify the document, page numbers involved, and location of the document (please attach copies, if possible).**

LABORATORY NOTEBOOK, DR. MICHAEL KOZICKI (6/2/00)

6. **When did you first successfully test this invention?** 6/23/00

7. **Identify any references, patent applications, or other publications of which you are aware and which you believe to be pertinent to this invention. Please attach a copy of each of these references, if available.**

SEE PATENT TREE

8. **If any proprietary material (e.g., cell line, antibody, plasmid, computer software, or chemical compound) btained from utsid y ur laboratory was used t develop this inventi n under a written transfer agreement (other than a normal purchasing agreement), please attach a c py f that agreement if available. If it is not available, please let us kn w if the document exists, and, possibly, where it may be.**

DISCLOSURE & PUBLICATION PLANS (EXTREMELY IMPORTANT)

Public disclosure affects patent rights – Please answer diligently

9. If you have disclosed this invention to non-ASU personnel (including research sponsor) then indicate when, under what circumstances, and to whom. NO PUBLIC DISCLOSURE

   a. orally: —

   b. in writing: —

   c. by actual use, demonstration, or posters: —

10. Have you submitted or do you plan to submit a report, abstract, paper, poster, or thesis relating to this invention for publication, for presentation at a conference, or to a research sponsor?

YES ☐ NO ☒

If yes, give details, including the actual or planned date of submission as well as expected time to acceptance. If a manuscript has been accepted, give the anticipated publication date. Append a copy of the latest draft manuscript available.

THE INVENTION ITSELF AND ITS UTILITY

11. A. Brief summary of the invention:
include novel features and advantages. Describe possible commercial applications

SEE ATTACHED SHEETS

B. Detailed description of the invention: Attach as many additional sheets as necessary.

SEE ATTACHED SHEETS

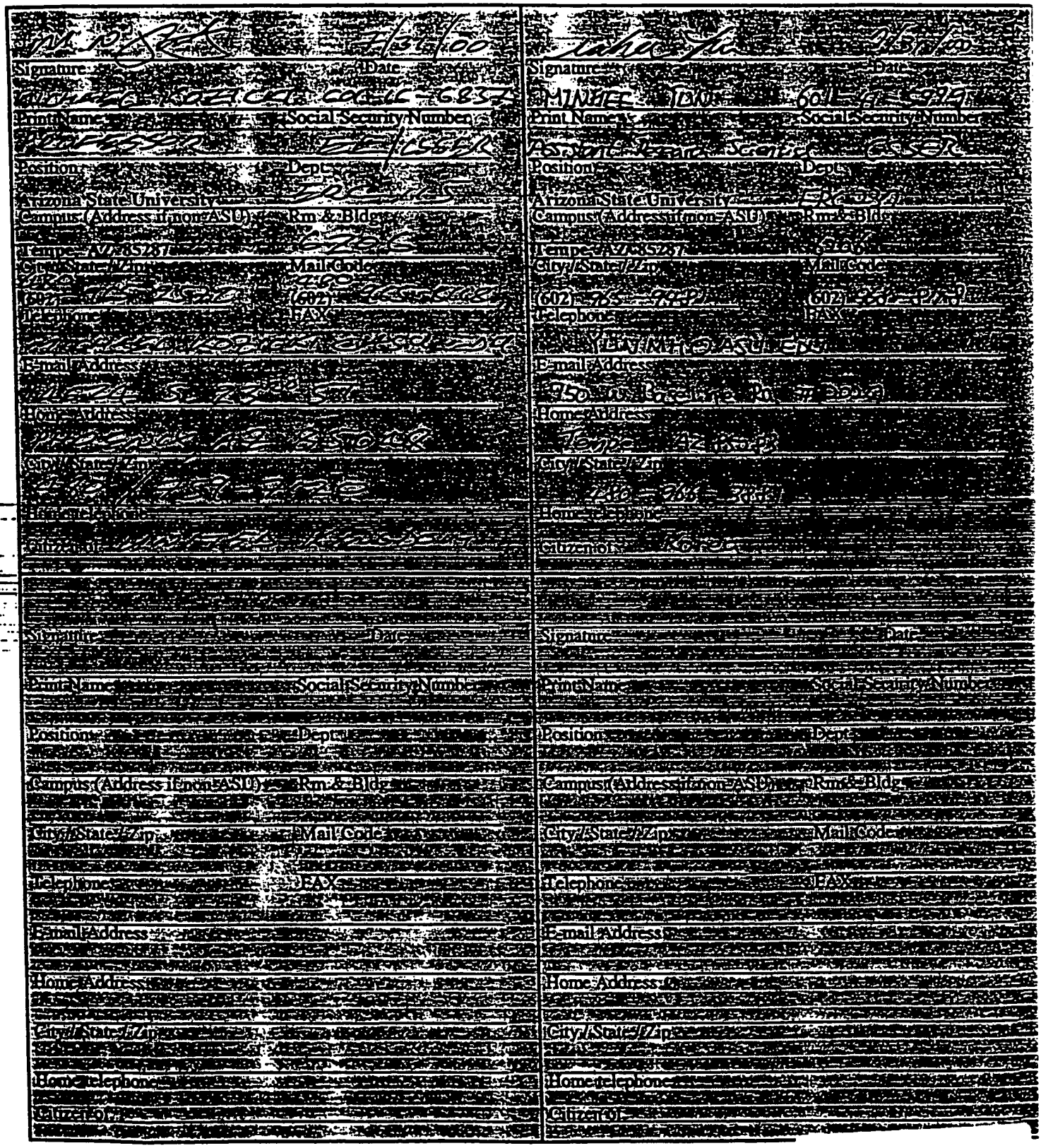
12. List companies you believe might be interested in using, developing or marketing this invention.

AXON TECHNOLOGIES CORPORATION

THIS INVENTION DISCLOSURE WILL NOT BE PROCESSED UNLESS THIS PORTION IS FILLED OUT COMPLETELY

13. Signatures, Names and addresses of Inventors

The undersigned agree t comply with ABOR policies on intellectual property and to execute suitable assignments of title if and when asked to do so.



Lower oxidizable layer – e.g. silver (required only if lower electrode is non-silver)
Solid solution 1 – e.g. silver in germanium selenide
Floating electrode – e.g. tungsten or other indifferent conductor
Solid solution 2 – e.g. silver in germanium selenide
Upper oxidizable layer – e.g. silver (required only if upper electrode is non-silver)
Upper electrode – e.g. silver or indifferent conductor

The horizontal variant would involve the same electrode options but deposited in a coplanar fashion on the surface of the solid solution such that the floating electrode is placed between the other two (connected) electrodes.

Basis of patent application and claims:

1. Use of a floating electrode in a PMC device or a derivative of such.
2. Use of oxidizable or indifferent electrode in this context.
3. Enhancement of data storage capabilty, allowing four easily read states (two bits) to be programmed in each cell of a PMC-like device.
4. Programming of the cell using polarity and current sequences.
5. Use of the device as a programmable anti-fuse element.
6. Formation of both horizontal and vertical variants of the device.

14. **Technically Qualified Witnesses (Tw Required)—invention discl sed to and understo d by:**

a) _____ _____
Signature Date

_____
Print Name

b) _____ _____
Signature Date

_____
Print Name

GROUP REVIEWED (DZICKI, MITKOVA, YUN, ABBROCCATI)

NOTE: ***When completed, the Disclosure and Record of Invention Form is an important legal document. Care should be taken in its preparation. Please refer to accompanying instructions. If you desire assistance, call the Office of Technology Collaborations & Licensing at 965-5670. Information contained in this document is maintained in confidence and normally will not be released to others except with attorney client privilege, to research sponsors as required by contract, under appropriate secrecy agreements, until a patent application is filed, the information is published, a determination not to file a patent application is made, or as may be required by law. The information contained should not be disclosed to others outside the University, except as described in section 9, without the approval of the ASU Office of Technology Collaborations & Licensing.***

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NOTE: University policies concerning intellectual property may be found at the following web site: http://researchnet.asu.edu/techcoll/ Click on "Resource Library"

Submit this form with ORIGINAL SIGNATURES directly to:

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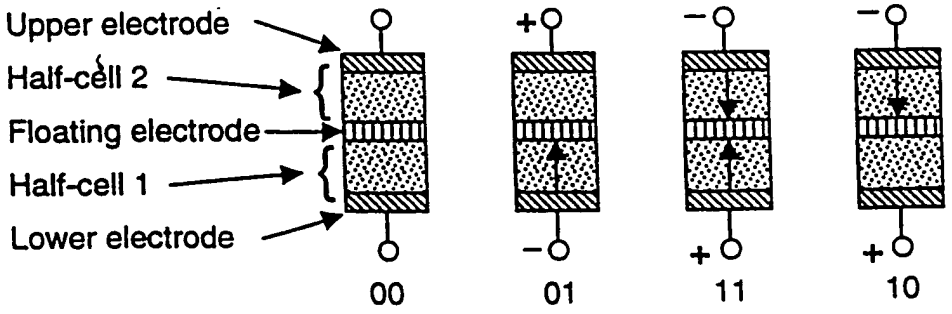
Bank One Building, 20 East University, Suite 201
Box 873511 Tempe, AZ 85287-3511

Effective 10/1/98

Programmable Metallization C ll with Floating Electrode
Multi-state programmable microelectronic device

The Floating Electrode Programmable Metallization Cell (FEPMC) uses an unconnected (floating) electrode between layers of a solid solution. The FEPMC operates in a similar fashion to the two electrode (asymmetric) PMC device in that an electrodeposit is made to form on or in a solid solution by the application of a small potential. The low resistance metallic electrodeposit shorts out the high resistivity glass and can be subsequently removed by the application of a reverse bias. This is how information is stored in the PMC device. The unique structure of the FEPMC allows four distinct and easily programmed states, which can represent two bits of binary information, to be stored in a single device.

The FEPMC structure essentially has five layers; lower electrode, solid solution 1, floating electrode, solid solution 2, and upper electrode. (Note that although this description pertains to a vertical device, a horizontal structure is also possible with all three electrodes being deposited on the surface of a thin layer of the solid solution.) If the floating electrode is the same as the metal in solution and the lower and upper electrodes are indifferent, or *vice-versa*, the entire structure may be thought of as two back-to-back PMC devices with a common electrode. Each "half-cell" is a PMC device in its own right but the common electrode is only supplied with electrons or ions via the solid solution layers and not by any other external connection. The full structure is shown schematically in the figure below.



Considering first the case of a structure with an oxidizable floating electrode, e.g., silver. In the unprogrammed state, the half cells have geometry and solution dependent impedances of Z_1 for half-cell 1 and Z_2 for half-cell 2. Typically, the solution layer thicknesses will be chosen so that Z_1 and Z_2 are distinctly different. The overall impedance of the FEPMC structure will be given by Z_1 in series with Z_2 and this may be used to represent state 00. If a voltage is applied such that the upp r electrode is positive with respect to the lower electrode and the magnitud is above that necessary to promote lectrodeposition in half-cell 1, an electrodeposit will form from the lower electrod to the floating lectrode as

shown by the arrow in the figure. Note that an electrodeposit will not grow in half-cell 2 as it is "reverse biased" and so will not support electrodeposition. The electrodeposit will change the impedance of half-cell 1 to Z_1', changing the overall impedance of the FEPMC and producing a value which may represent state 01. The current or charge limit will set the magnitude of the change and should be chosen sufficiently low so that it is possible to subsequently erase the electrodeposit with a reasonable current.

If the polarity is now reversed (with a similar low current level), most of the applied bias will be dropped across the high resistance solution of half-cell 2 rather than across half-cell 1, and so an electrodeposit will form from the top electrode to the floating electrode without dissolving the connection in half-cell 1, as shown in the figure. The impedance of half-cell 2 now becomes Z_2' and the overall impedance is Z_1' in series with Z_2'. This device impedance can be used to represent state 11.

Once both half-cells are shorted, either electrodeposit can be dissolved by applying a sufficient (reverse) bias across the appropriate half-cell. However, if the upper electrode is once again made negative with respect to the lower but using a higher current limit which allows sufficient reverse bias across half-cell 1, only this cell will be erased (see figure). Half-cell 1 will therefore return to Z_1 and the overall device impedance will be Z_1 in series with Z_2', representing state 10. The entire four state sequence is summarized in the table below.

Seq.#	Polarity	Current limit	Z half-cell 1	Z half-cell 2	State/value
1	Sub-threshold	Zero	Z_1	Z_2	00
2	Upper + Lower –	Low	Z_1'	Z_2	01
3	Upper – Lower +	Low	Z_1'	Z_2'	11
4	Upper – Lower +	High	Z_1	Z_2'	10

It is possible to return to state 11 from state 10 simply by applying a low current limit bias to regrow the electrodeposit in half-cell 1 (upper +, lower -). From state 11, dissolving the electrodeposit in half-cell 2 by applying a high current limit bias such that the upper electrode is again positive with respect to the lower will take the device to state 01. Finally, if state 00 is now to be attained, a short current pulse must be applied to thermally dissolve the electrodeposit in half-cell 1. This can be done with the same polarity as the half-cell 1 write but with a current limit which is high enough to cause localized heating of the electrodeposit. This will increase the metal concentration in the half-cell but this excess metal can be removed electrically from the cell by plating it back onto the floating electrode (this will happen when half-cell 2 is written to, i.e., when the upper electrode is negative with respect to the lower). This sequence is summarized in the table below.

Seq #	Polarity	Current limit	Z half-cell 1	Z half-cell 2	State/value
4	Existing state	-	Z_1	Z_2'	10
5	Upper + Lower –	Low	Z_1'	Z_2'	11
6	Upper + Lower –	High	Z_1'	Z_2	01
7	Upper + Lower –	Thermal	Z_1	Z_2	00

Note that other sequences are possible (as are other definitions of the various states represented by the half-cell impedances). For example, it is possible to go from state 00 to either state 01 or state 10, depending on the write polarity chosen. Similarly, it is possible to go from state 11 to either state 10 or state 01. It is also possible to go from state 11 to state 00 by the application of a current pulse (in either direction) which is high and short enough to thermally dissolve the electrodeposits in both half-cells simultaneously.

In addition to storing information in digital form, the FEPMC can also be used as a noise-tolerant low energy anti-fuse element for use in field programmable gate arrays (FPGAs) and field configurable circuits and systems. Most physical anti-fuse technologies require large currents and voltages to make a permanent connection. The need for such high energy state-switching stimuli is generally considered to be somewhat beneficial as this reduces the likelihood of the anti-fuse accidentally forming a connection in electrically noisy situations. However, the use of high voltages and large currents on chip represent a significant problem as all components in the programming circuits have to be sized accordingly and the high energy consumption reduces battery life in portable systems.

The FEPMC represents a low energy anti-fuse solution which is relatively noise immune. The device can only be closed (fully shorted to the lowest impedance state) if a pulse of one polarity is followed by one of the opposite polarity. This eliminates the likelihood of switching due to unipolar voltage spikes, which are common in digital and mixed signal integrated circuits.

Two vertical configurations of the FEPMC are possible, both being formed by multi-layer deposition. Note that the vertical FEPMC can be fabricated so that it is entirely contained within a via in a dielectric layer. For an oxidizable floating electrode, the layer sequence would be as follows:

Lower electrode – e.g. tungsten or other indifferent conductor
Solid solution 1 – e.g. silver in germanium selenide
Floating electrode – e.g. silver
Solid solution 2 – e.g. silver in germanium selenide
Upper electrode – e.g. tungsten or other indifferent conductor

For a non-oxidizable floating electrode, the layer sequence would be as follows:

Lower electrode – e.g. silver or an indifferent conductor